Analog Integrated Circuits and Signal Processing, 19, 241–254 (1999)

A New CMOS Programmable Balanced Output Transconductor and Application to a Mixed Mode Universal Filter Suitable for VLSI

SOLIMAN A. MAHMOUD AND AHMED M. SOLIMAN

Electronics and Communication Engineering Deptartment, Cairo University, Egypt

Received August 28, 1997; Revised January 21, 1998; Accepted February 2, 1998

Abstract. A new CMOS programmable balanced output transconductor (BOTA) is introduced. The BOTA is a useful block for continuous-time analog signal processing. A new CMOS realization based on MOS transistors operating in the saturation region is given. Application of the BOTA in realizing a mixed mode universal filter using six BOTAs and two grounded capacitors is also introduced. The filter's gain can be adjusted simply by varying the amplitude of a transconductance through its control voltage without affecting ω_0 and Q of the filter. Also, the Q of the filter can be adjusted by a single transconductor independent of ω_0. PSpice simulation results for the BOTA circuit and for the universal filter are also given.

Key Words: transconductors, filters

1. Introduction

The programmable balanced output transconductor (BOTA) is a useful building block for continuous-time analog signal processing. Based on the BOTA circuit, MOS floating and grounded resistors, balanced output integrators, MOS-C filters with balanced outputs and the active realization of passive filters with minimum number of the BOTAs can be built [1]. Several realizations for the CMOS transconductors with a single or multiple outputs have been introduced in the literature [2–12]. The realizations given in [2–6] are based on using a differential stage with MOS transistors operating in the saturation region. The CMOS transconductors given in [7,8] are based on the use of MOS transistors operating in the nonsaturation region. The use of both a differential stage and MOS transistors operating in the nonsaturation region to realize CMOS transconductors are given in [9,10]. The CMOS transconductors given in [11,12] are based on the use of the composite transistor which has one NMOS and one PMOS placed in series. The composite transistor was proposed to solve the problem of biasing the source of the MOS transistor (low input impedance node) by providing two high input impedance terminals to control the current through the device. Unfortunately, the use of the composite transistor has the disadvantage of high equivalent threshold voltage that limits the operation of the circuit to high supply voltage and reduces the dynamic range [13]. The proposed CMOS realization of the BOTA avoids the use of composite transistors by using two voltage buffers. The application of the single output transconductors in realizing integrators, inductors, frequency dependent negative resistors are given in [14] and also in realizing filters are given in [14,15]. The application of the multiple output transconductors to realize tunable continuous time filters are given in [16]. A direct application of the balanced output transconductor is in the implementation of voltage controlled floating resistors [17]. The realization given in [1] provides a CMOS transconductor with a balanced output current based on the use of a wide input range differential CMOS transconductor in cascade with a voltage controlled MOS grounded resistor [18] and a balanced output transconductor stage.

In this paper, a new CMOS realization of a balanced output transconductor based on transistors operating in the saturation region is given. The proposed balanced output transconductor can be programmed using a control voltage which allows to compensate for process parameter spreads in automatically tuned filters. The BOTA, whose symbol is

shown in Fig. 1, has two input voltages and provides two balanced output currents through the two output terminals. The structure of the proposed transconductor is based on the current linearization of two basic NMOS transistors by generating a suitable biasing voltages in term of the input voltages to bias the sources of the basic transistors. The application of the BOTA in realizing a universal mixed mode filter is given. This universal active filter employs six BOTAs and two grounded capacitors. The filter has infinite input impedance. It realizes highpass, bandpass, lowpass, allpass and notch with mixed voltage and current responses. The filter's gain can be adjusted simply by varying the amplitude of a certain transconductance through its control voltage without affecting ω_0 or Q of the filter. Also, the Q of the filter can be adjusted by a single transconductor independent of ω_0.

In Section 2, the realization of the programmable CMOS balanced output transconductor is presented. In Section 3, the realization of the MOS-C universal filter is given. PSpice simulation results for the transconductor circuit indicating the linearity range and for the universal filter to verify the analytical results are also given.

2. The Proposed Balanced Output Transconductor Circuit

The proposed CMOS balanced output transconductor circuit is shown in Fig. 2. The matched transistors M1 to M4 are the basic transistors and their gate voltages are the input voltages to the transconductor. Transistors M5 to M16 form the biasing circuit for the sources of the transistors M1 to M4. The remaining transistors perform the current transfer to the output ports of the transconductor circuit. All the transistors are assumed to be operating in the saturation region with their sources connected to their substrate/bulk. The MOS drain current in the saturation region is given by:

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \tag{1}$$

where

$$K = \mu C_{\text{ox}}(W/L) \tag{2}$$

W/L is the transistor aspect ratio.
C_{ox} is the gate-oxide capacitance per unit area.
μ is the electron mobility.
V_T is the threshold voltage (assumed equal for all MOS transistors).
From Fig. 2

$$I_0 = I_1 - I_2 \tag{3}$$

where

$$I_1 = \frac{K}{2}(V_1 - V_a - V_T)^2 \tag{4}$$

and

$$I_2 = \frac{K}{2}(V_2 - V_b - V_T)^2 \tag{5}$$

Therefore

$$I_0 = \frac{K}{2}(V_1 + V_2 - V_a - V_b - 2V_T)(V_1 - V_2 + V_b - V_a) \tag{6}$$

From the biasing circuit realized from M5 to M11, expression for the biasing voltage V_b in terms of V_1 can be obtained as follows:

The currents of the transistors M5, M6 and M7 are equal and are given, respectively, by:

$$I_5 = \frac{K_5}{2}(V_1 - V_x - V_T)^2 \tag{7}$$

$$I_6 = \frac{K_6}{2}(V_x - V_b - V_T)^2 \tag{8}$$

$$I_7 = \frac{K_7}{2}(V_C - V_T)^2 \tag{9}$$

From the above equations and with $K_5 = K_6 = 4K_7$, the biasing voltage V_b is given by:

$$V_b = V_1 - V_C - V_T \tag{10}$$

The transistors M11 and M5 (M16 and M12) together with the biasing current from M10 (M15) form a negative feedback action which provides the

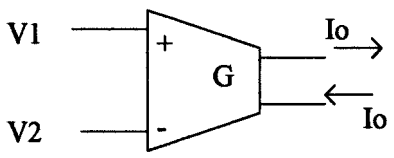

Fig. 1. The symbol of the BOTA.

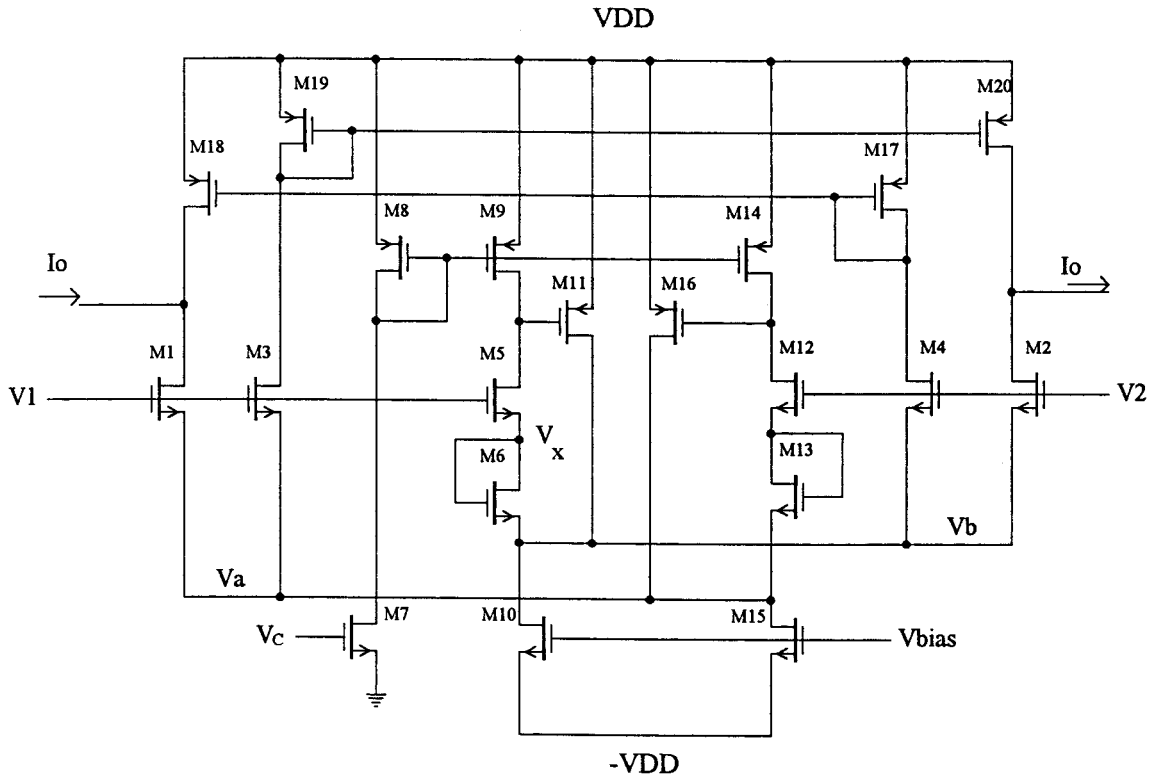

Fig. 2. The CMOS circuit of the BOTA.

necessary current from the output without changing the voltage (voltage buffer).

Similarly, the expression of the biasing voltage V_a can be obtained from the biasing circuit formed from the transistors M12 to M16 and is given by:

$$V_a = V_2 - V_C - V_T \tag{11}$$

From (10), (11) and (6) one gets

$$I_0 = 2KV_C(V_1 - V_2) \tag{12}$$

Therefore, the CMOS circuit shown in Fig. 2 operates as a balanced output transconductor, with a programmable transconductance G which is controlled by the control voltage V_C and is given by:

$$G = 2KV_C \tag{13}$$

The performance of the proposed BOTA circuit was verified by PSpice simulations with supply voltages $\pm$ 3.3 V and with the SPICE parameters given in Table 1 and the aspect ratios given in Table 2.

The output current of the BOTA versus V_1 for various values of V_2 with V_1 and V_2 scanned from $-$ 1.5 V to 1.5 V and with $V_C = 2.285$ V is shown in Fig. 3(a). The output current of the BOTA versus V_1 when V_2 is grounded and V_C taken as a control parameter and scanned from 1.4 to 3 V is shown in Fig. 3(b). The magnitude and phase responses of the BOTA's output current which look flat up to 10 MHz are shown in Figs. 4(a) and 4(b). PSpice results in the output-referred and input referred noise voltage spectral densities for the BOTA when terminated by 1 KΩ is shown in Fig. 4(c). The power Supply Rejection Ratio (PSRR) from the positive supply to the output is 42.55 dB and from the negative supply to the output is 71.5 dB . The Total Harmonic Distortion (THD) is less than 0.25% for 100 KHz 1 V peak-to-peak sinusoidal input. The mismatches between the basic MOS transistors M1 to M4 produce harmonic distortion and offset of the transfer curve therefore the input range for the same previous THD is decreased

Table 1.

Model parameters set for 2 µm CMOS Technology (obtained through MOSIS)
.MODEL NMOS NMOS LEVEL = 2 LD = 0.225112U TOX = 405.000001E − 10
NSUB = 2.256421E + 15 VTO = 0.77227 KP = 4.954000E − 05 GAMMA = 1.0151 PHI = 0.6
UO = 581 UEXP = 0.217142 UCRIT = 115146 DELTA = 1.360440 VMAX = 68535.3
XJ = 0.250000U NFS = 2.85E + 12 NEFF = 1 NSS = 1.000000E + 10 TPG = 1.000000
RSH = 27.020000 CGDO = 2.873845E − 10 CGSO = 2.880845E − 10 CGBO = 3.840832E − 10
CJ = 4.100000E − 04 MJ = 0.4650 CJSW = 4.803300E − − 10 MJSW = 0.351 PB = 0.800000
.MODEL PMOS PMOS LEVEL = 2 LD = 0.177432U TOX = 405.000001E − 10
NSUB = 3.956006E + 15 VTO = − 0.74048 KP = 2.526000E − 05 GAMMA = 0.4251 PHI = 0.6
UO = 299.253 UEXP = 0.1933 UCRIT = 5462.67 DELTA = 0.91285 VMAX = 29720.9
XJ = 0.250000U NFS = 1.00E + 11 NEFF = 1 NSS = 1.000000E + 10 TPG = − 1.000000
RSH = 107.40000 CGDO = 2.262940E − 10 CGSO = 2.268940E − 10 CGBO = 3.471103E − 10
CJ = 1.898000E − 04 MJ = 0.439556 CJSW = 2.267600E − 10 MJSW = 0.207266 PB = 0.700000

Table 2.

MOS Transistors	Aspect Ratio (W μm/Lμm)
M1, M2, M3, M4	5/12
M5, M6, M12, M13	16/4
M7	4/4
M8, M9, M10, M14, M15, M16, M17, M18, M19, M20	400/4

consequently. For $V_{DD} = -V_{SS} = 3.3\text{V}$ and $V_C = 2.285\text{V}$, the input common mode range for THD less than 0.25% at 100 KHz is $\pm$ 1.5 V. When the mismatch of (M1, M2) and (M3, M4) is increased to 5%, 10% and 20%, the input common mode range for the same THD is reduced to $\pm$ 1.38 V, $\pm$ 1.29 V and $\pm$ 0.825 V respectively.

3. The Proposed Mixed Mode BOTA-C Universal Filter

Fig. 5 represents the new filter circuit which realizes second order lowpass, bandpass, highpass, allpass and notch voltage and current transfer functions. The circuit includes six BOTA's and two grounded capacitors, which makes the filter suitable for VLSI implementation. Similar filter structure is first introduced in [19] but using current conveyors. By direct analysis, the voltage transfer functions are obtained as:

$$\frac{V_{LP}}{V_i} = \frac{\frac{G_i G_1 G_2}{G_5 C_1 C_2}}{D(S)} \tag{14}$$

$$\frac{V_{BP}}{V_i} = -\frac{S\frac{G_i G_1}{G_5 C_1}}{D(S)} \tag{15}$$

$$\frac{V_{HP}}{V_i} = \frac{S^2\frac{G_i}{G_5}}{D(S)} \tag{16}$$

and the mixed mode transfer functions are given by:

$$\frac{I_{LP}}{V_i} = \frac{\frac{G_i G_1 G_2 G_3}{G_5 C_1 C_2}}{D(S)} \tag{17}$$

$$\frac{I_{BP_1}}{V_i} = -\frac{S\frac{G_i G_1 G_2}{G_5 C_1}}{D(S)}, \qquad \frac{I_{BP_2}}{V_i} = -\frac{S\frac{G_i G_1 G_4}{G_5 C_1}}{D(S)} \tag{18}$$

$$\frac{I_{HP_1}}{V_i} = \frac{S^2\frac{G_i G_1}{G_5}}{D(S)}, \qquad \frac{I_{HP_2}}{V_i} = \frac{S^2 G_i}{D(S)} \tag{19}$$

where

$$D(S) = S^2 + S\frac{G_1 G_4}{G_5 C_1} + \frac{G_1 G_2 G_3}{G_5 C_1 C_2} \tag{20}$$

From the above equation, the ω_0 and Q of the filter are given by:

$$\omega_0 = \sqrt{\frac{G_1 G_2 G_3}{G_5 C_1 C_2}}, \qquad Q = \frac{1}{G_4}\sqrt{\frac{G_5 G_2 G_3 C_1}{G_1 C_2}} \tag{21}$$

The ω_0 and the Q sensitivities to all circuit components are very low (≤ 1). As seen from equations (14), (15), (16) and (20), the DC gain (LP response), the gain at ω_0 (BP response) and the high frequency gain (HP response) are given, respectively, by:

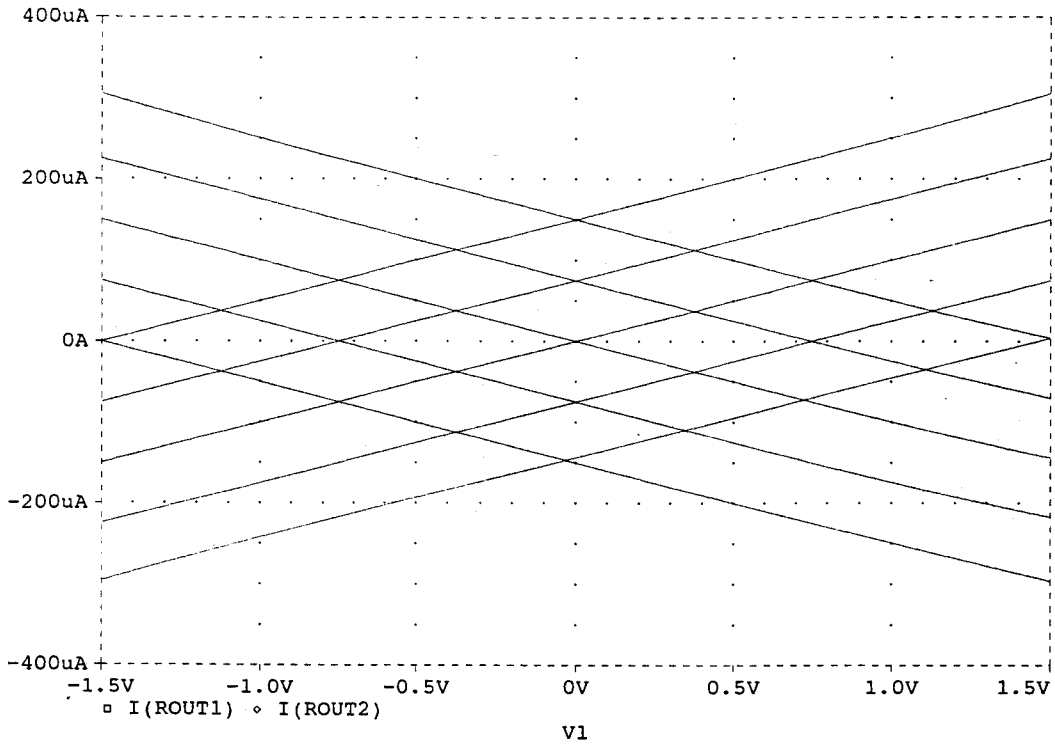

Fig. 3(a). The I-V characteristics of the output currents of the BOTA.

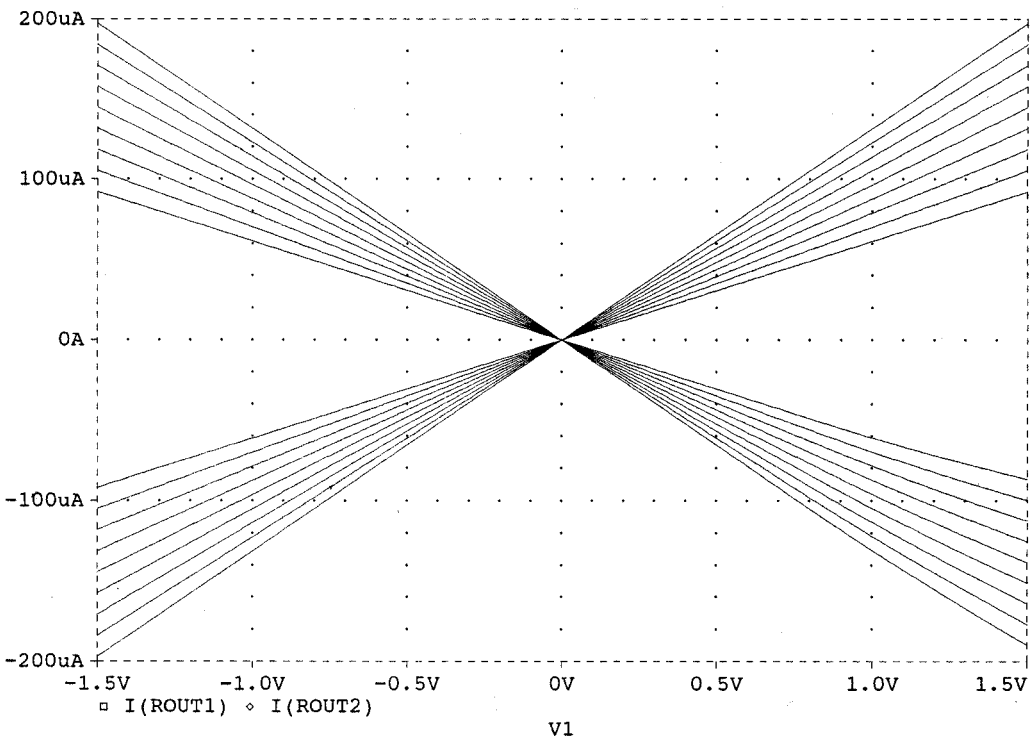

Fig. 3(b). The I-V characteristics of the output currents of the BOTA with Vc as a parameter.

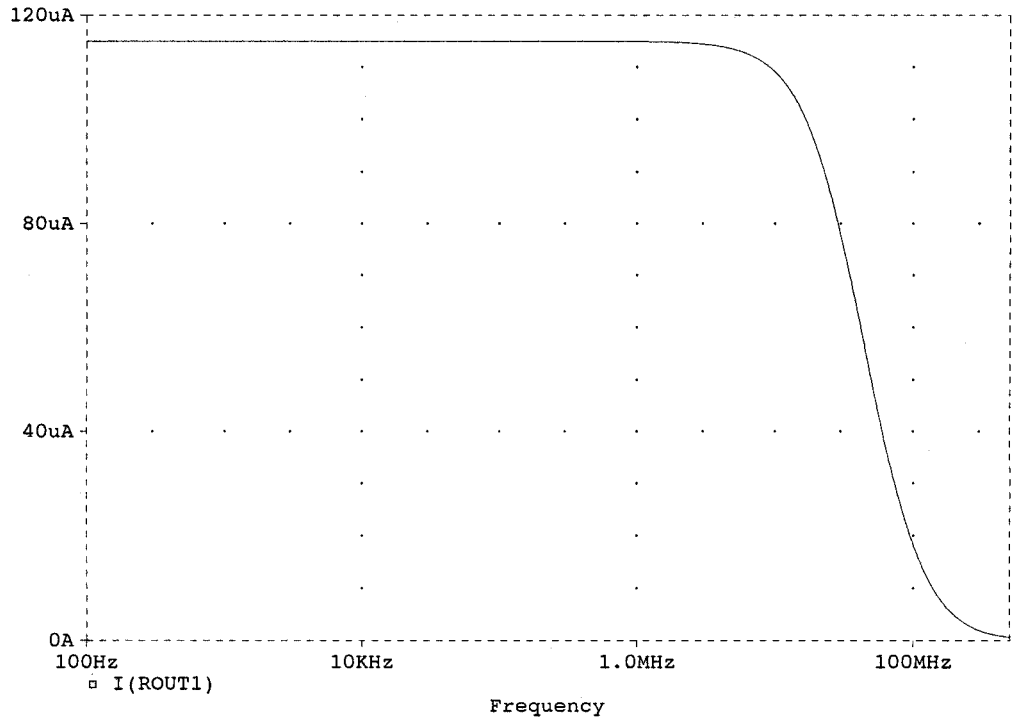

Fig. 4(a). The magnitude response of the proposed BOTA.

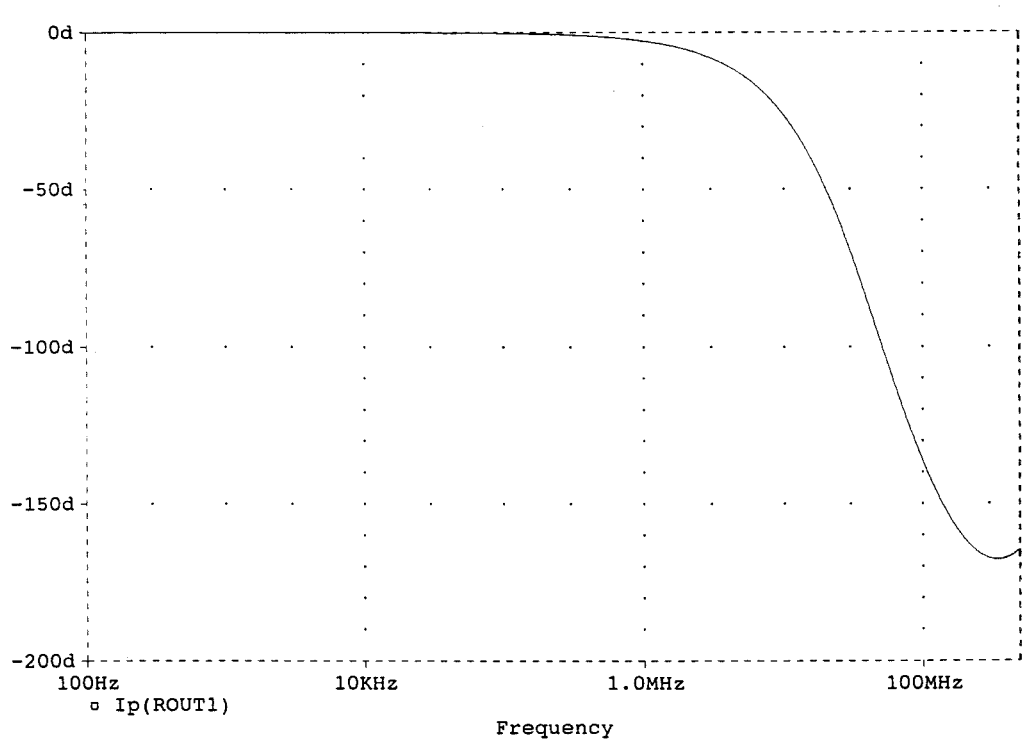

Fig. 4(b). The phase response of the proposed BOTA.

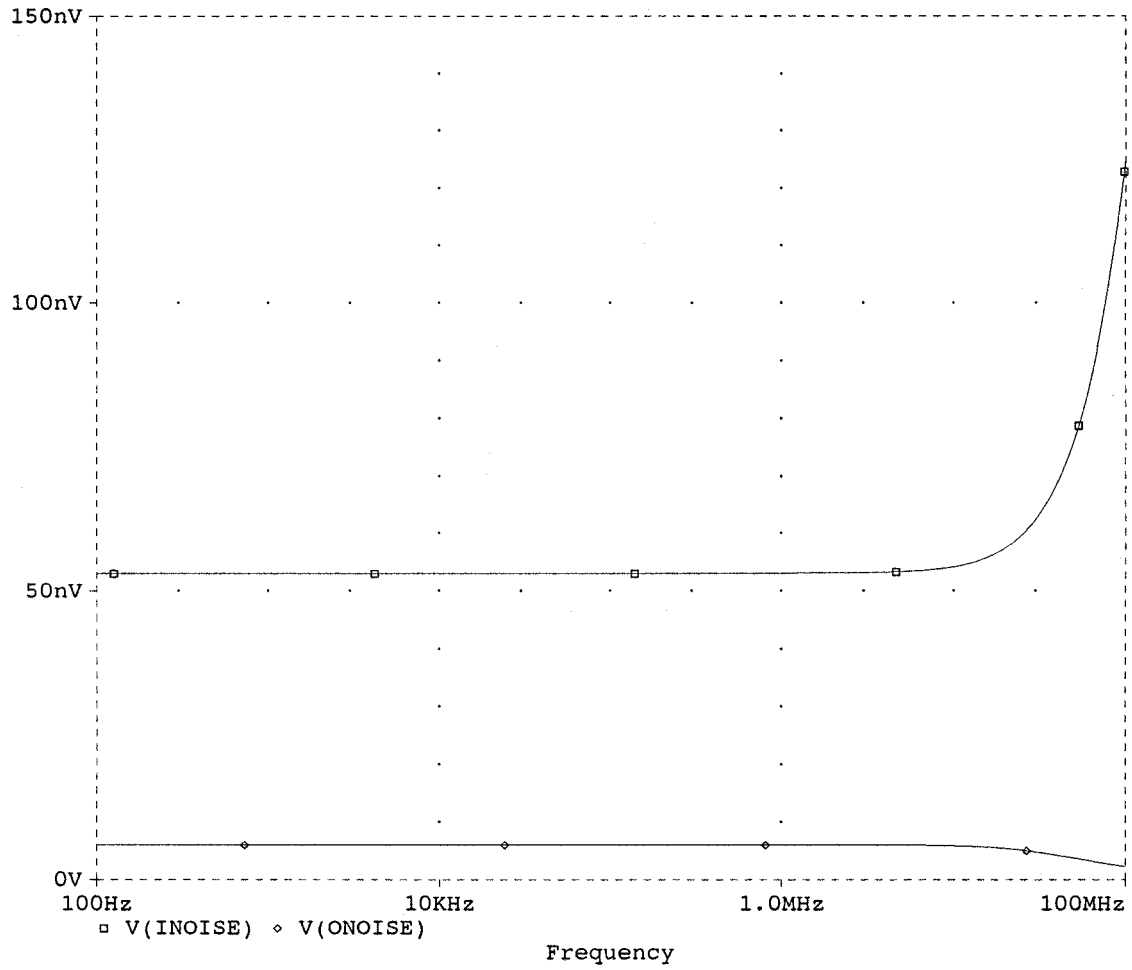

Fig. 4(c). The output-referred and input referred noise voltage spectral densities for the BOTA when terminated by 1 KΩ.

$$T_{\mathrm{VLP}}(0) = \frac{G_i}{G_3} \tag{22}$$

$$|T_{\mathrm{VBP}}(\omega_0)| = \frac{G_i}{G_4} \tag{23}$$

$$T_{\mathrm{VHP}}(\infty) = \frac{G_i}{G_5} \tag{24}$$

From the above four equations, it is seen that the transconductance G_i controls the gain of the filter without affecting ω_0 and Q.

For specified ω_0, Q and the gain at ω_0 of the BP response, the design equations are given by:

$$C_1 = C_2 = C \tag{25}$$

$$G_1 = G_5 \tag{26}$$

$$G_2 = G_3 = \omega_0 C \tag{27}$$

$$G_4 = \frac{\omega_0 C}{Q} \tag{28}$$

$$G_i = G_4 |T_{\mathrm{VBP}}(\omega_0)| \tag{29}$$

It is seen that the transconductance G_4 controls Q of the filter without affecting ω_0 of the circuit.

If the circuit is to be designed for a specific DC gain, then equation (29) should be replaced by the following equation:

$$G_i = G_2 T_{\mathrm{VLP}}(0) \tag{30}$$

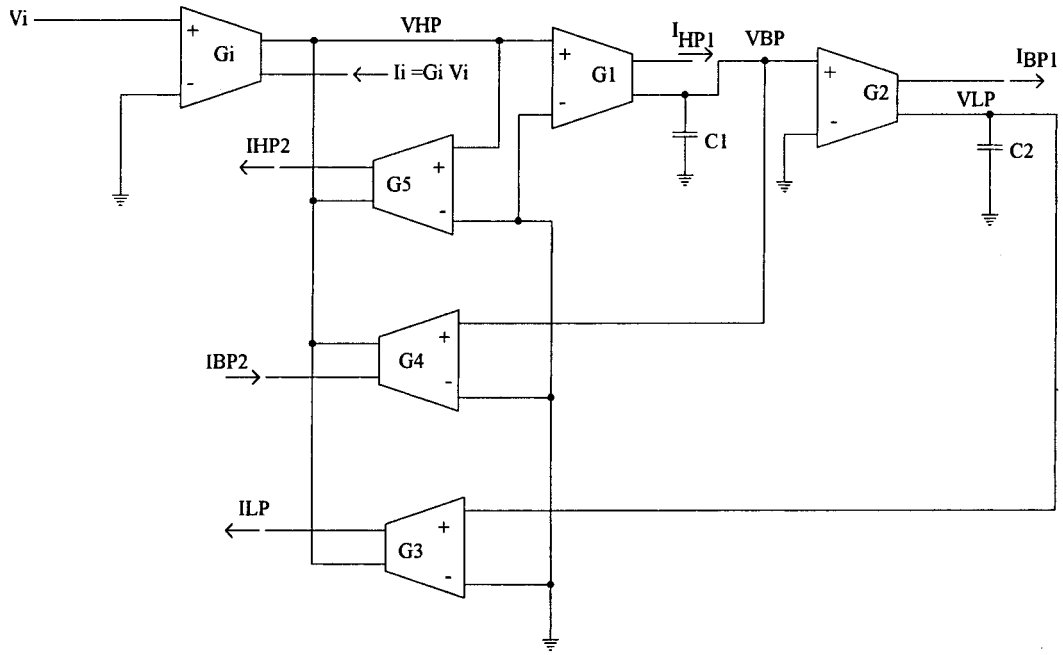

Fig. 5. The proposed BOTA-C mixed mode universal active filter.

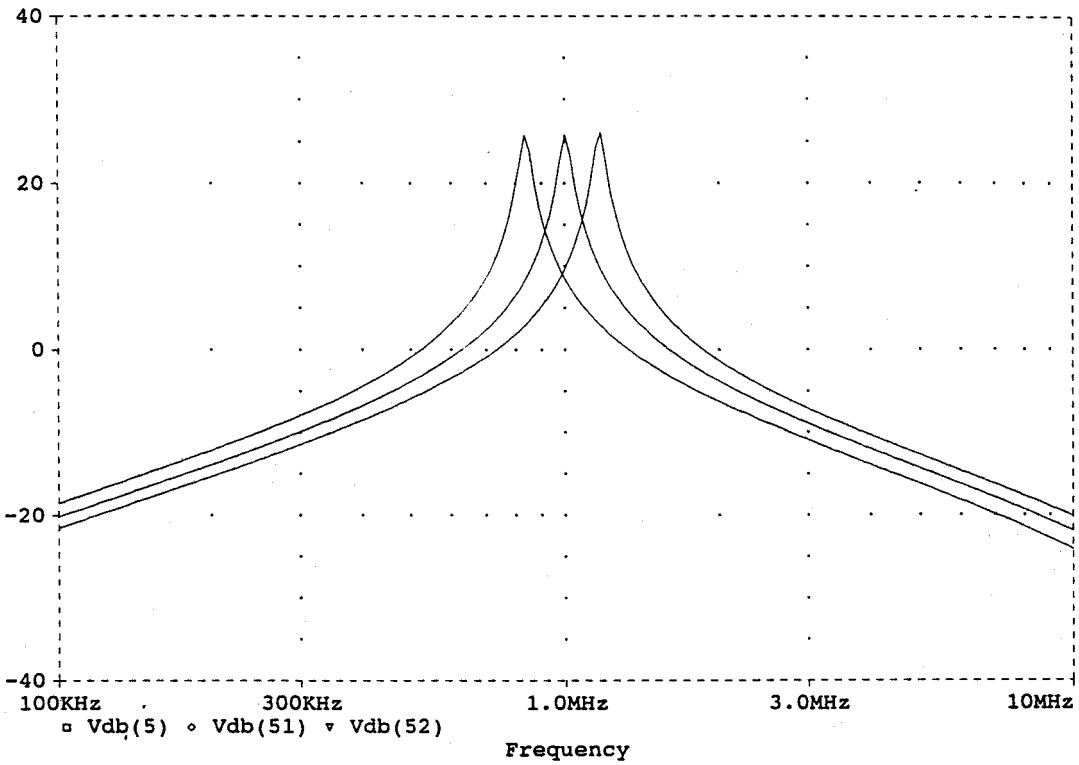

Fig. 6. The magnitude response of the voltage mode bandpass output.

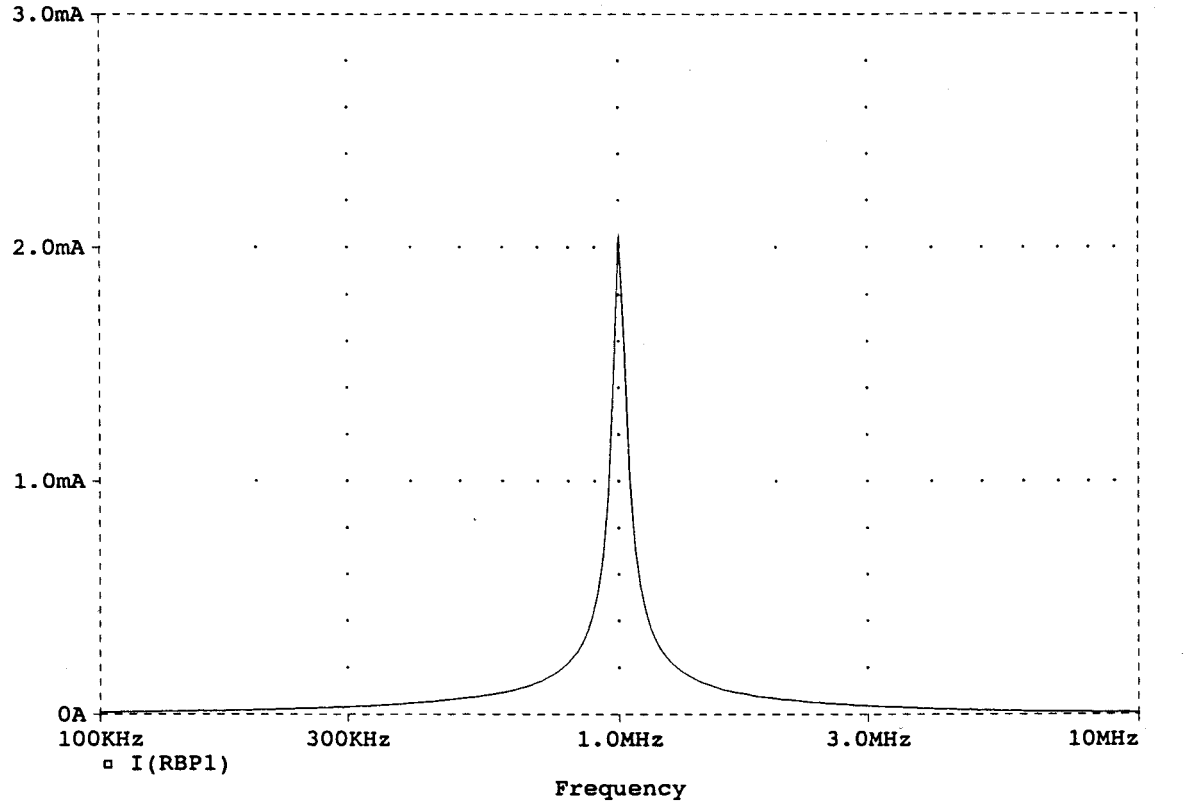

Fig. 7. The bandpass output current.

Also if the circuit is to be designed for a specific highpass frequency gain, then equation (29) should be replaced by the following equation:

$$G_i = G_1 T_{\mathrm{VHP}}(\infty) \tag{31}$$

Note that, there are two alternative ways to realize a mixed mode notch current response, if the output current is taken by adding I_i and I_{BP2} or adding I_{LP} and I_{HP2}, therefore the mixed mode transfer function of the notch response is given by:

$$\begin{aligned}\frac{I_{\mathrm{notch}}}{V_i} &= \frac{I_i + I_{\mathrm{BP2}}}{V_i} = \frac{I_{\mathrm{LP}} + I_{\mathrm{HP2}}}{V_i} \\ &= G_i \frac{S^2 + \frac{G_1 G_2 G_3}{G_5 C_1 C_2}}{S^2 + S\frac{G_1 G_4}{G_5 C_1} + \frac{G_1 G_2 G_3}{G_5 C_1 C_2}}\end{aligned} \tag{32}$$

Note also that, the allpass current response can be obtained by adding I_{LP}, I_{BP1} and I_{HP1}, therefore the mixed mode transfer function of the allpass response is given by:

$$\frac{I_{\mathrm{AP}}}{V_i} = \frac{I_{\mathrm{LP}} + I_{\mathrm{BP1}} + I_{\mathrm{HP1}}}{V_i} = \frac{G_i G_1}{G_5} \frac{S^2 - S\frac{G_2}{C_1} + \frac{G_2 G_3}{C_1 C_2}}{S_2 + S\frac{G_1 G_4}{G_5 C_1} + \frac{G_1 G_2 G_3}{G_5 C_1 C_2}} \tag{33}$$

With the condition:

$$G_1 = G_5 \text{ and } G_2 = G_4 \tag{34}$$

Note that, from equations (32), (33) and (34), the gain of the notch and allpass responses equal to G_i.

PSpice simulations for the circuit of Fig. 5 with $C_1 = C_2 = 15.9\,\mathrm{pF}$, and $G_i = G_5 = G_1 = G_2 = G_3 = 20\,\mathrm{G}_4 = 2\,\mathrm{KV}_C\,\mu\mathrm{AV}^{-1}$ to obtain a bandpass response with electronically tunable center frequency around $f_0 = 1\mathrm{MHz}$, $Q = 20$, and $|T_{\mathrm{VBP}}(\omega_0)| = 20$. Fig. 6 shows the magnitude of the voltage mode output of the bandpass filter. The center frequency is controlled by scanning the control voltage V_C from 2 to 2.8 V with 0.4 V step and with the transconductance parameter $K = \frac{125}{6}\,\mu\mathrm{AV}^{-2}$. Fig. 7 shows the bandpass

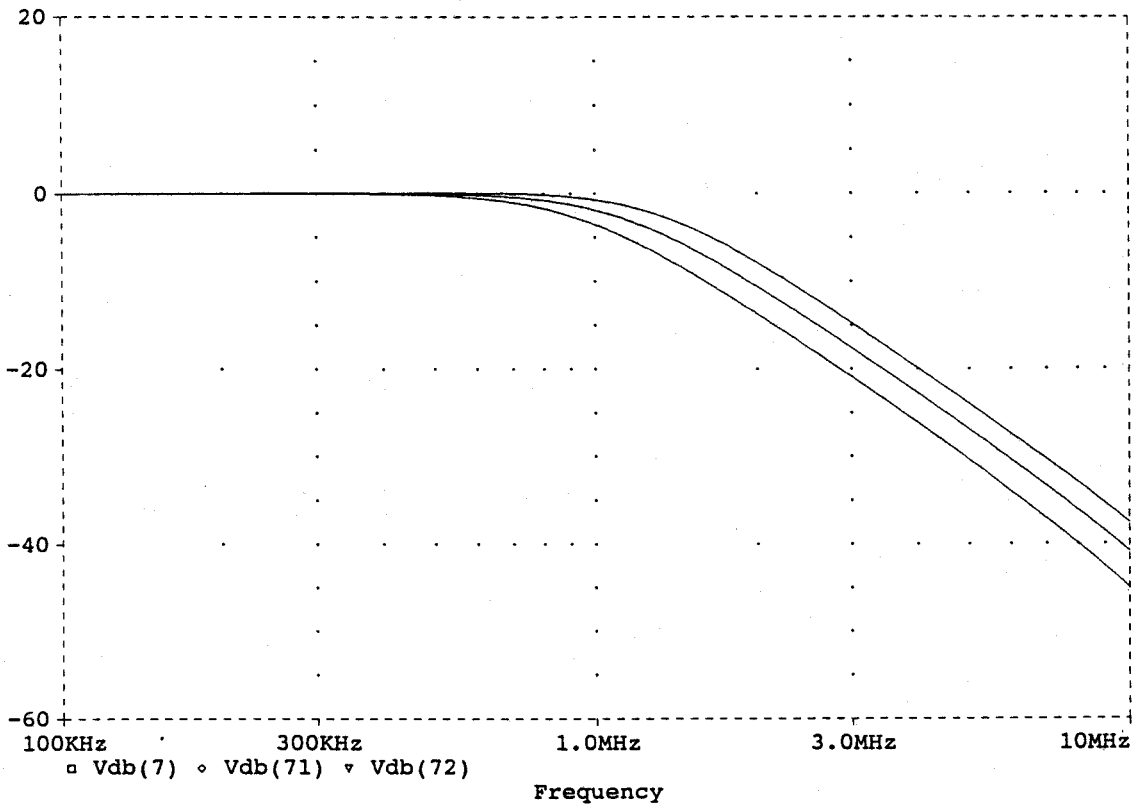

Fig. 8. The magnitude response of the voltage mode lowpass output.

output current for V_C equal to 2.4 V. Where the current is measured in a load resistance of 1 KΩ.

Simulation results for the same circuit with $C_1 = C_2 = 15.92\,\text{pF}$, $G_i = G_5 = G_1 = G_2 = G_3 = 0.707\,G_4 = 2\,\text{KV}_C\mu\text{AV}^{-1}$ to obtain a maximally flat lowpass and highpass responses designed for a DC and high frequency gain of 1 and with a tunable f_0 around 1 MHz. Fig. 8, Fig. 9 show the amplitude of the voltage mode lowpass and highpass response. The cutoff frequency is controlled by scanning the control voltage V_C from 2 to 2.8 V with 0.4 V step and with the transconductance parameter $K = \frac{125}{6}\mu\ \text{AV}^{-2}$. Fig. 10 and Fig. 11 show the lowpass and the highpass output currents for $V_C = 2.4\,\text{V}$.

Simulation results for the circuit of Fig. 5 to obtain a notch characteristics with $C_1 = C_2 = 15.9$ pF and $G_i = G_5 = G_1 = G_2 = G_3 = 2\,G_4 = 100\mu\text{AV}^{-1}$ are shown in Fig. 12 where the notch response when I_{BP2} is added to I_i or I_{LP} to I_{HP2} in a load resistance of 1 KΩ.

Simulation results for the circuit of Fig. 5 to obtain an allpass characteristics with $C_1 = C_2 = 15.9$ pF and $G_i = G_5 = G_1 = G_2 = G_3 = G_4 = 100\,\mu\text{AV}^{-1}$ are shown in Fig. 13 indicating phase characteristics of the allpass filter when I_{LP}, I_{BP1} and I_{HP1} are added together in a load resistance of 1 KΩ.

4. Conclusions

A new CMOS programmable balanced output transconductor has been proposed. Application of the BOTA to realize a universal filter is given. This universal filter provides the following advantages: low passive and active sensitivities, suitable for VLSI implementation using only grounded capacitors, the control of the Q and the filter's gain are independent of ω_0. PSpice simulation results for the proposed CMOS-BOTA and for the filter circuit are obtained which confirm the analytical results. To ensure

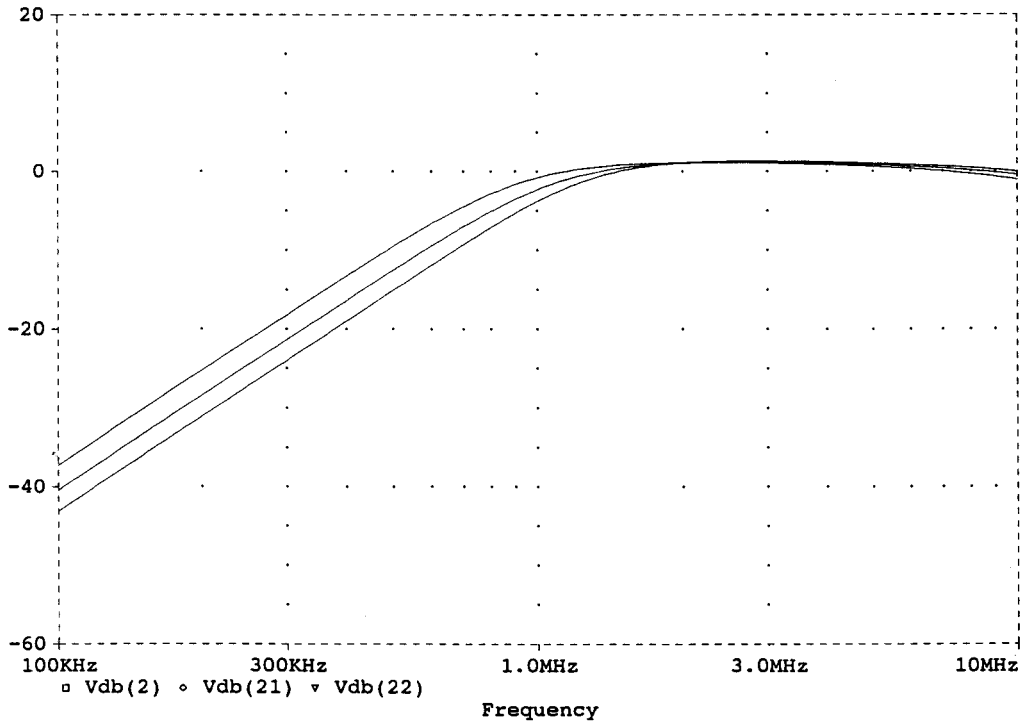

Fig. 9. The magnitude response of the voltage mode highpass output.

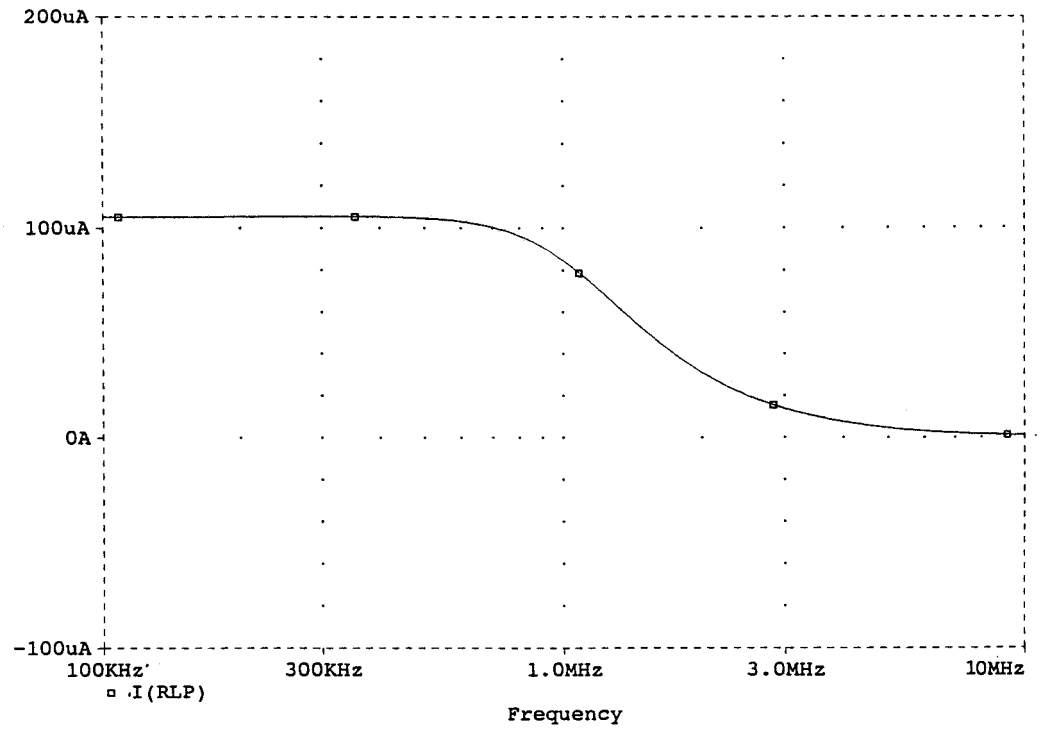

Fig. 10. The lowpass output current.

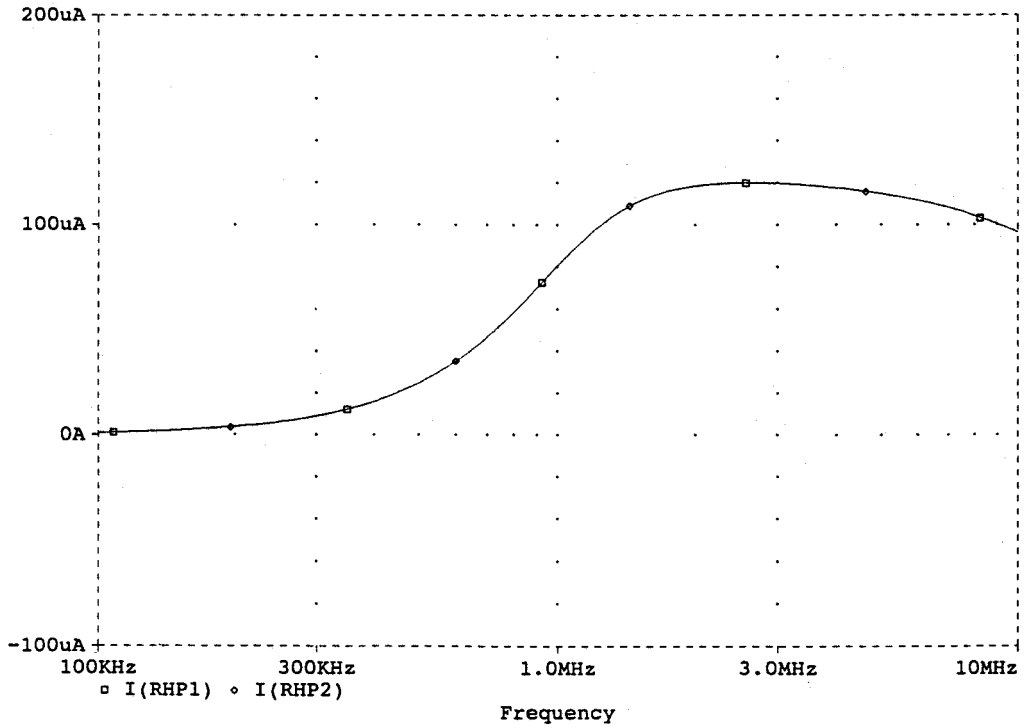

Fig. 11. The highpass output current.

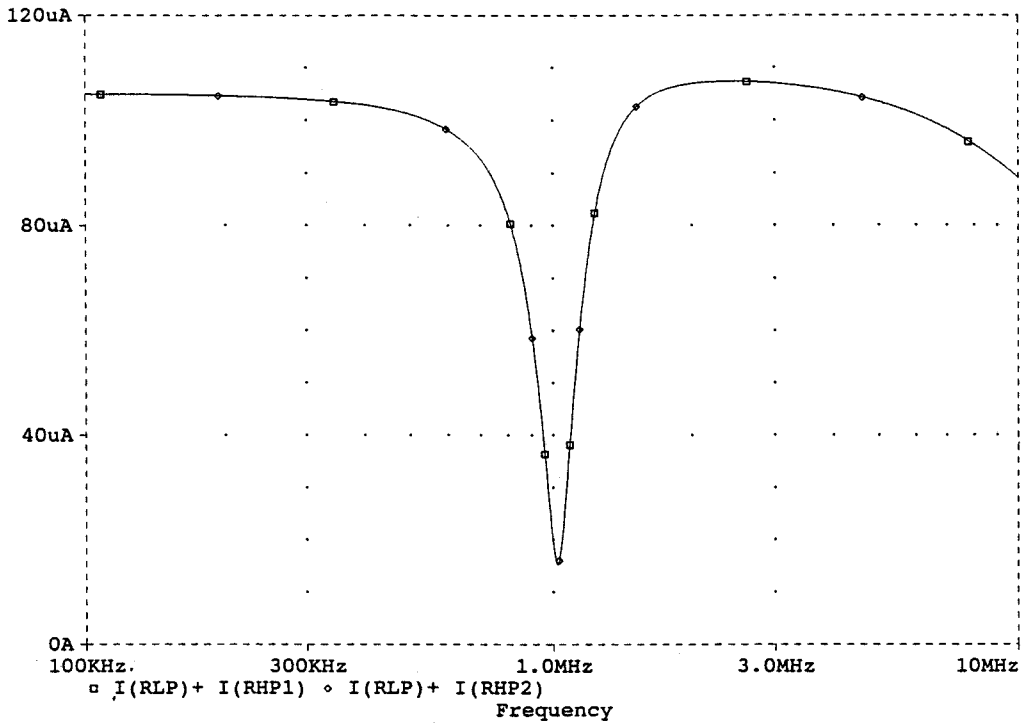

Fig. 12. The magnitude response of the notch output current.

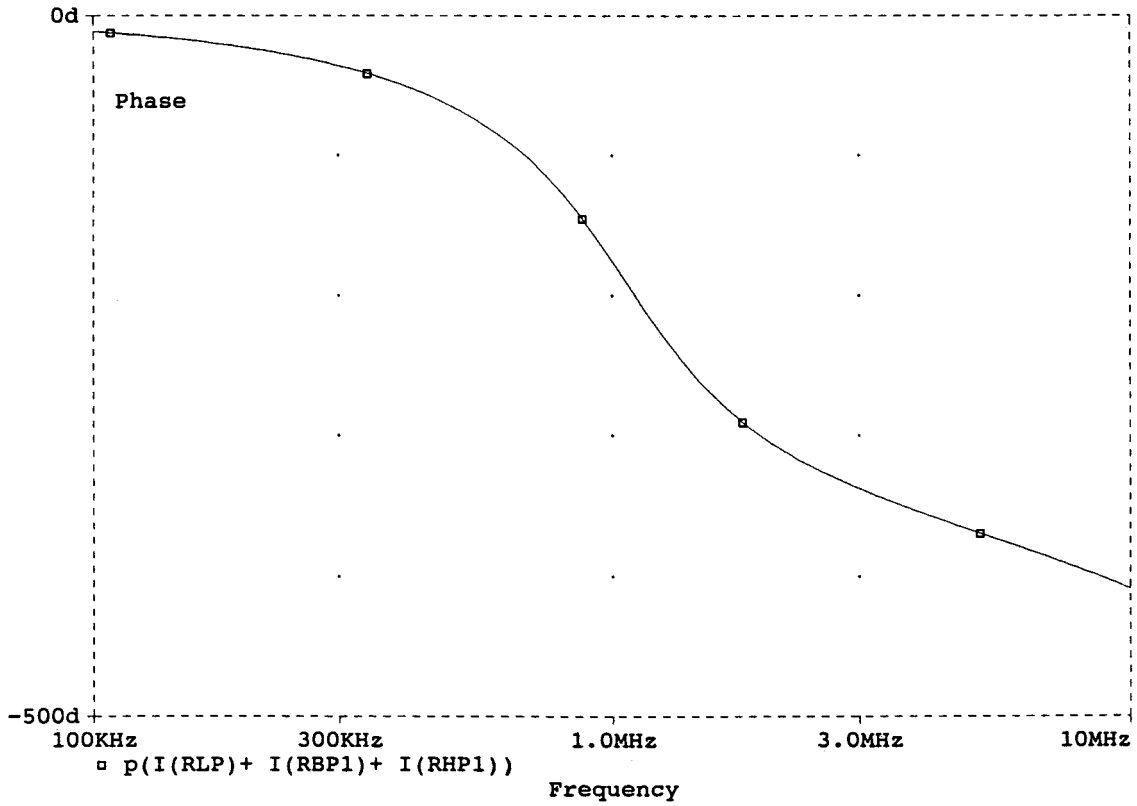

Fig. 13. The phase response of the allpass output current.

balanced output operation of the BOTA a common mode feedback circuit is needed.

References

1. S. A. Mahmoud and A. M. Soliman, ''A CMOS programmable balanced output transconductor for analog signal processing.'' *International Journal of Electronics* 82(6), 605–620, 1997.
2. A. Nedungadi and T. R. Viswanthan, ''Design of linear CMOS transconductor elements.'' *IEEE Trans. Circuits Syst.* CAS-31, 891–894, 1984.
3. J. Silva-Martines, M. S. J. Steyaert, and W. Sansen, ''A large signal very low-distoration transconductor for high frequency continuous-time filters.'' *IEEE J. Solid-State Circuits* SC-26, 946–955, 1991.
4. Y. T. Wang, F. Lu, and A. A. Abidi, ''A 12.5 MHz CMOS continuous time band pass filter.'' *IEEE Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* 198–199, 1989.
5. F. Krummencher and N. Joehl, ''A 4 MHz CMOS continuous-time filter with on chip automatic tuning.'' *IEEE J. Solid-State Circuits* SC-23, 750–758, 1989.
6. J. L. Pennock, ''CMOS triode transconductor for continuous-time active integrated filters.'' *Electron. Lett.* 21, 817–818, 1985.
7. S. L. Wang, ''Novel drain-biased transconductance building blocks for continuous-time active filters.'' *Electron. Lett.* 25, 100–101, 1989.
8. U. Gatti, F. Maloberti, G. Palmisano, and G. Torelli, ''CMOS triode-transistor transconductor for high-frequency continuous-time filters.'' *IEE Proc. Circuits, Devices and Syst.* 141, 462–468, 1994.
9. Y. Tsividis, Z. Czarnul, and S. C. Fang, ''MOS transconductors and integrators with high linearity.'' *Electron. Lett.* 22, 245–246, 1986.
10. V. Gopinathan, Y. Tsividis, K. Tan, and P. K. Hester, ''Design consideration for high frequency continuous-time filters and implementation of antialiasing filter for digital video.'' *IEEE J. Solid-State Circuits* SC-25, 1368–1378, 1990.
11. E. Seevinck and R. Wassenaar, ''A versatile CMOS linear transconductor/ square-law function circuit.'' *IEEE J. Solid-State Circuits* SC-22, 366–377, 1987.
12. S. -C. Huang and M. Ismail, ''Linear tunable COMFET transconductor.'' *Electron. Lett.* 29, 459–461, 1993.
13. A. Hyogo, C. Hwang, M. Ismail, and K. Sekine, ''LV/LP CMOS square-law Composite Transistors for Analog VLSI Applications.'' *1st Analog VLSI workshop proceedings* Columbus, Ohio 139–143, 1997.

14. R. L. Geiger and E. Sanchez-Sinencio, ''Active filter design using operational transconductance amplifiers: A tutorial.'' *IEEE Circuits Devices Magazine* 1, 20–32, 1985.
15. P. V. Ananda Mohan, ''Generation of OTA-C filter structures from active RC filter structures.'' *IEEE Trans. Circuits Syst.* 37, 656–659, 1990.
16. V. I. Prodanov and M. M. Green, ''Improved biquad structures using double-output transconductance blocks for tunable continuous-time filters.'' *Analog Integrated Circuits and Signal Processing* 13, 233–240, 1997.
17. S. A. Mahmoud, H. O. Elwan, and A. M. Soliman, ''Generation of CMOS voltage controlled floating resistors.'' *Microelectronics Journal* 28, 627–640, 1997.
18. S. A. Mahmoud, H. O. Elwan, and A. M. Soliman, ''Grounded MOS resistor.'' *Electronic Engineering* 22–24, 1997.
19. A. M. Soliman, ''Current conveyors steer universal filter.'' *Circuits and Devices Magazine* 11, 45–46, 1995.

Soliman A. Mahmoud was born in Cairo, Egypt, on September 27, 1971. He received the B.S. degree with honors and the M.S. degree from the Electronics and Communications Department, Cairo University, Egypt in 1994 and 1996 respectively. He is a T.A. in Cairo University, Fayoum Branch. Dr. Mahmoud received his Ph.D. degree in March 1999. His research interests include analog CMOS circuit design, filtering and applications suitable for VLSI.

Ahmed M. Soliman was born in Cairo, Egypt, on November 22, 1943. He received the B.S. degree with honors from Cairo University, Cairo, Egypt, in 1964, the M.S. and Ph.D. degrees from the University of Pittsburgh, Pittsburgh, PA, in 1967 and 1970, respectively, all in electrical engineering.

He is currently Professor and Chairman, Electronics and Communications Engineering Department, Cairo University, Egypt.

From 1985–1987, Dr. Soliman served as Professor and Chairman of the Electrical Engineering Department, United Arab Emirates University, and from 1987–1991 he was the Associate Dean of Engineering at the same university.

He has held visiting academic appointments at San Francisco State University, Florida Atlantic University and the American University in Cairo.

He was a visiting scholar at Bochum University, Germany (Summer 1985) and with the Technical University of Wien, Austria (Summer 1987).

In 1977, Dr. Soliman was decorated with the First Class Science Medal, from the President of Egypt, for his services to the field of engineering and engineering education.