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New Four-Quadrant CMOS Current-Mode and Voltage-Mode Multipliers

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Abstract. In this paper, a four-quadrant current-mode multiplier based on a new squarer cell is proposed. The multiplier has a simple core, wide input current range with low power consumption, and it can easily be converted to a voltage-mode by using a balanced output transconductor (BOTA) [1]. The proposed four-quadrant current-mode and voltage-mode multipliers were confirmed by using PSPICE simulation and found to have good linearity with wide input dynamic range. For the proposed current-mode multiplier, the static power consumption is 0.671 mW, the maximum power consumption is 0.72 mW, the input current range is ± 60 μA, the bandwidth is 31 MHz, the input referred noise current is 46 pA/$\sqrt{\text{Hz}}$, and the maximum linearity error is 3.9%. For the proposed voltage-mode multiplier, the static power consumption is 1.6 mW, the maximum power consumption is 1.85 mW, the input voltage range is $\pm$1V from $\pm$1.5V supply, the bandwidth is 25.34 MHz, the input referred noise voltage is 0.85 μV/$\sqrt{\text{Hz}}$, and the maximum linearity error is 4.1%.

Key Words: multiplier, current mode, voltage mode, transconductance

1. Introduction

A multiplication of two signals is one of the most important operations in analog signal processing. The multiplier is used not only as computation building block but also as a programming element in systems such as filters, neural networks, mixers, and modulators in communication systems [2]. Several MOS four-quadrant multipliers have been reported but all can be categorized into two groups based on its MOS operating region, linear and saturation [3]. The operation of the multiplier only in linear or saturation region limits the input-voltage range, so the multiplier presented in [2] has wider input-voltage range as a result of operation in linear and saturation regions complementally.

The analog circuit design using the current-mode approach has recently gained considerable attention. This stems from its inherent advantages of wide bandwidth, high slow rate, low power consumption, and simple circuitry [4, 5]. This is clearly obvious in the four-quadrant current-mode multipliers presented in [6, 7] which based on current squarer cells.

In this paper a novel four-quadrant current-mode multiplier that has simple core circuit based on a simple novel squarer cell will be proposed. Although this circuit has design trade off among the input current range, the output current dynamic range, and the power consumption, it can be designed to operate with low supply voltage ($\pm$1.5 V) under low power consumed with acceptable dynamic ranges for both input and output currents. The proposed current-mode multiplier circuit is presented in Section 2. In Section 3, balanced output transconductor (BOTA) circuit given in [1] is used to drive the proposed four-quadrant current-mode multiplier. The four-quadrant voltage-mode multiplier has attractive performance that it has very good linearity with wide differential-input voltage range.

The proposed circuits of four-quadrant current-mode and voltage-mode multipliers are simulated using CMOS 0.5 μm technology.

2. CMOS Current-Mode Multiplier

The proposed four-quadrant current mode multiplier is based on a novel squarer cell. The design of the squarer cell and the complete circuit of the multiplier will be given in the following sub-sections.

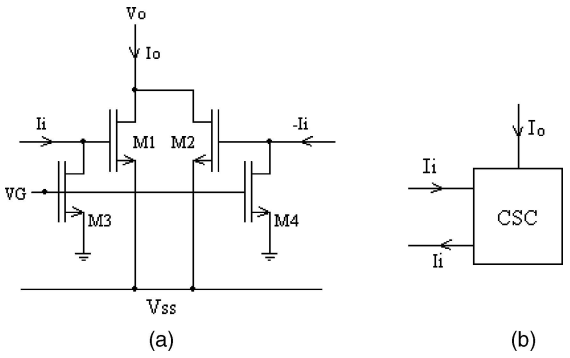

Fig. 1. (a): CMOS realization of the proposed squarer cell, (b): Symbol of the proposed squarer cell.

2.1. Proposed Current-Mode Squarer Cell

The proposed current-mode squarer cell is shown in Fig. 1. The symbol of the squarer cell is shown in Fig. 1(b) and its CMOS realization is shown in Fig. 1(a). The circuit consists of four transistors; M_1 and M_2 are operated in the saturation region and assumed to be matched, and M_3 and M_4 are operated in the linear region and assumed to be matched also. M_3 and M_4 are equivalently representing grounded resistors with resistance value approximately given by:

$$R = \frac{1}{K_3(V_G - V_T)} \tag{1}$$

where K_3 is the transconductance parameter of transistors M_3 and M_4, $K_3 = \mu C_{\text{ox}}(W/L)_3$, μ is the mobility of the carrier, C_{ox} is the gate capacitance per unit area, W is the channel width, L is the channel length, V_T is the threshold voltage, and V_G is the biasing gate voltage. As the biasing gate voltage (V_G) increased, the above approximation is held better.

From Fig. 1(a), assuming that both I_i and $-I_i$ are available, the output current of the squarer I_o is given by:

$$I_O = I_{D1} + I_{D2} \tag{2}$$

Where I_{D1} and I_{D2} are the drain currents of the saturated transistors M_1 and M_2 and are given by:

$$I_{D1} = \frac{K_1}{2}\left(R^2 I_i^2 - 2RI_i(V_{\text{SS}} + V_T) + (V_{\text{SS}} + V_T)^2\right) \tag{3}$$

$$I_{D2} = \frac{K_1}{2}\left(R^2 I_i^2 + 2RI_i(V_{\text{SS}} + V_T) + (V_{\text{SS}} + V_T)^2\right) \tag{4}$$

Where, K_1 is the transconductance parameter of transistors M_1 and M_2. From the above equations, the output current can be written as:

$$I_O = I_{\text{OFF}} + K_S I_i^2 \tag{5}$$

Where I_{OFF} is the output offset current (at $Ii = 0$A) and is given by:

$$I_{\text{OFF}} = K_1(V_{\text{SS}} + V_T)^2 \tag{6}$$

And K_S is the squarer gain and is given by:

$$K_S = K_1 R^2 \tag{7}$$

From equations (6) and (7), I_{OFF} will be controlled by the transistors aspect ratio $(W/L)_1$ and by the biasing voltage (V_{SS}). The squarer gain K_S will be controlled independently by the resistance R which can be controlled by the voltage V_G and $(W/L)_3$.

2.2. Design Considerations of the Proposed Squarer Circuit

In this section, the design considerations to optimize the input current range, the output current dynamic range, static power dissipation and the output voltage (V_O) that can be driven by the circuit will be discussed.

Assuming that M_3 and M_4 are carefully designed to operate in the linear region with equivalent grounded resistance R, The operation of the squarer circuit is restricted by the saturation condition of the MOS transistors M_1 and M_2. The following conditions can be driven for symmetrical input current range ($|I_{i-\min.}| = I_{i-\max.}$).

$$|RI_i| \le |V_{\text{SS}} + V_T| \tag{8}$$

$$V_{O-min.} = |V_{\text{SS}}| - 2V_T \tag{9}$$

Using the above two equations in addition to equations (5) to (7), the input current range ($|I_i|_{\max}$), and the output current dynamic range ($I_{O-\text{DR}}$) are given by:

$$|I_i| \le \frac{|V_{\text{SS}} + V_T|}{R} \tag{10}$$

$$I_{O-\text{DR}} = K_1 R^2 (I_i)^2 \le I_{\text{OFF}} \tag{11}$$

The static power dissipation is linearly proportional to $I_{OFF,}$ so trade off among the input current range, the output current dynamic range, and the static power dissipation is clearly obvious.

2.3. Current-Mode Multiplier

The block diagram of the proposed four-quadrant current-mode multiplier is shown in Fig. 2(a). The multiplier circuit consists of four similar squarer cells and a current-subtraction circuit. The CMOS realization of the current-mode multiplier is shown in Fig. 2(b). Transistors (M_{1A} to M_{4D}) are the squarer cells, the first generation current conveyor (CCI) consisting of transistors M_5 to M_8 represents a current subtraction circuit to obtain a single ended output current I_O, which is given by:

$$I_O = I_{O1} - I_{O2} \tag{12}$$

Where,

$$I_{O1} = I_{Oa} + I_{Ob} = I_{\text{OFF}} + I_{\text{OFF}} + K_S(I_X + I_Y)^2 \tag{13}$$

$$I_{O2} = I_{Oc} + I_{Od} = I_{\text{OFF}} + K_S(I_X)^2 + I_{\text{OFF}} + K_S(I_Y)^2 \tag{14}$$

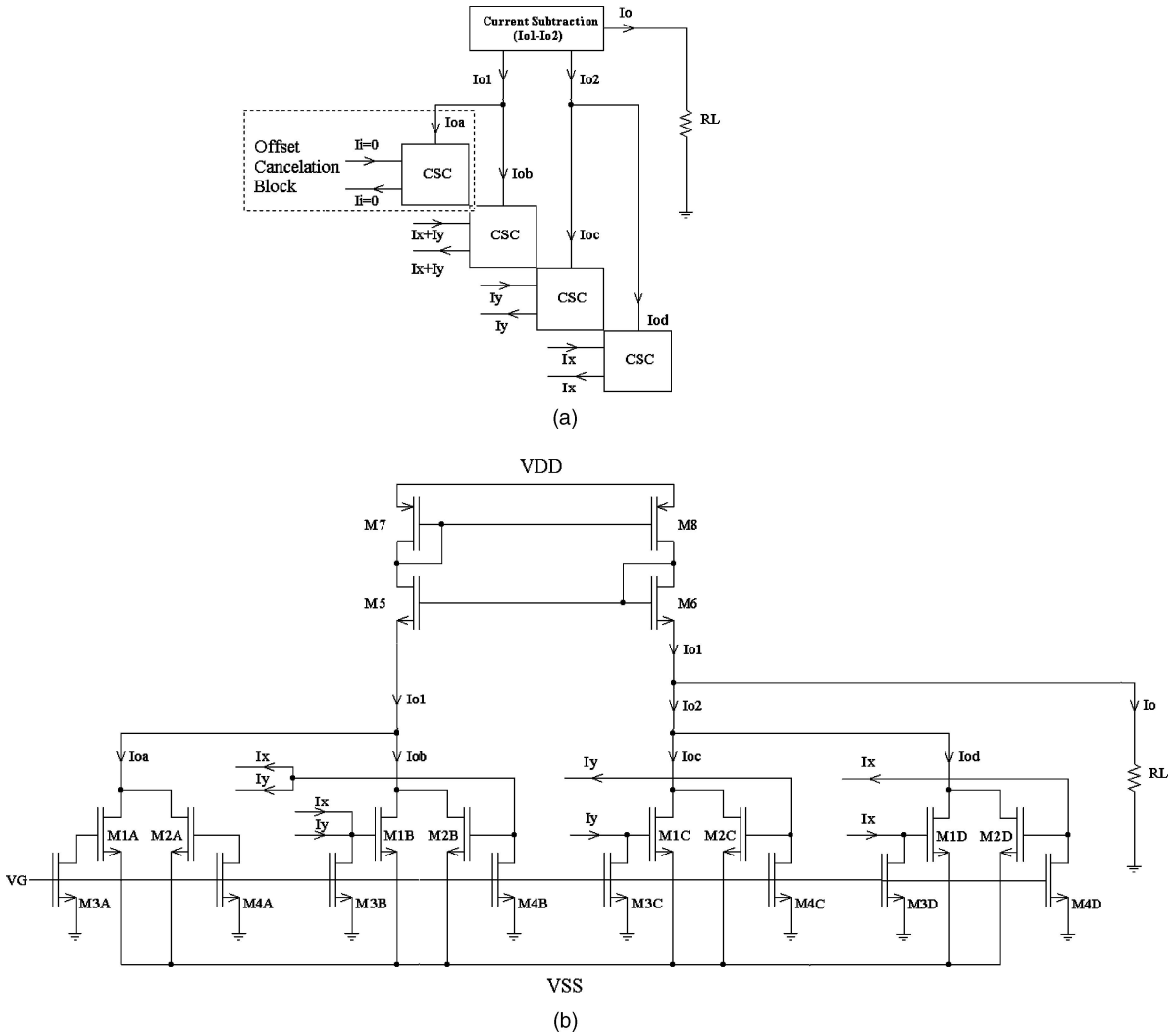

Fig. 2. (a): Block diagram of the proposed current-mode multiplier, (b): CMOS realization of the proposed current-mode multiplier.

Therefore, the output current of the multiplier (I_O) is given by:

$$I_O = (2K_1R^2)I_X I_Y \tag{15}$$

This topology achieves multiplication and simultaneously cancels out all higher order components of I_X and I_Y. The gain of the multiplier is $2K_1R^2$ where K_1 is the transconductance parameter of the saturated transistors M_{1A} to M_{2D} and R is the equivalent grounded resistance of the linear transistors M_{3A} to M_{4D}.

2.4. Channel Length Modulation Effect

The drain current of the MOS transistor with the effect of channel length modulation is given by:

$$I_D = \frac{K}{2}\,(V_{\rm GS}-V_T)^2(1+\lambda V_{\rm DS}) \tag{16}$$

where, λ is the channel length modulation parameter. By taking channel length modulation effect into consideration, the output current of the basic squarer cell given by equation (5) can be rewritten as follows:

$$I_O = (I_{\rm OFF} + K_S I_i^2)(1+\lambda V_{\rm DS}) \tag{17}$$

Where, V_{DS} is the drain-to-source voltage of both M_1 and M_2 in Fig. 1.

Since the current subtraction in the current-mode multiplier is realized using CCI circuit as shown in Fig. 2, all squarer cells forming the current-mode multiplier have the same $V_{\rm DS}$. Therefore, the output current of the multiplier given by equation (15) can be rewritten as follows:

$$I_O = (2K_1R^2)I_X I_Y(1+\lambda V_{\rm DS}) \tag{18}$$

The channel length modulation effect can be reduced using longer channel length transistors to reduce λ.

2.5. Mismatching Effect

The derivation of the output current equation of the basic squarer cell (equation (5)), and hence the output current equation of the multiplier (equation (15)), was based on the assumption that the transistors forming the squarer cell are matched. In this subsection, the mismatching effect will be discussed.

Referring to the current squarer circuit of Fig. 1, assume that M_1 has transconductance parameter equals K_1, and M_2 has transconductance parameter equals $K_1 + \Delta K_1$. Then, equation (5) can be rewritten as follows:

$$I_O = \left(I_{\rm OFF} + K_S I_i^2\right) + \nabla K_1[(RI_i)^2 + 2RI_i(V_{\rm SS}+V_T) + (V_{\rm SS}+V_T)^2] \tag{19}$$

Since the complete current-mode multiplier is constructed by repeating this modular current squarer cell, assuming that the mismatching in all the squarer cells is the same and substituting equation (19) in equations (12–14), the output current equation of the multiplier can be rewritten as follows:

$$I_O = (2K_1R^2)I_X I_Y + (\nabla K_1 R^2)I_X I_Y = I_{\rm O\,match.} + \nabla I_O \tag{20}$$

where, $I_{\rm O\,match}$ is the output current in the matched case. Therefore, the percentage error of the output current due to mismatching effect is constant and equal half of the percentage of mismatching as given in the following equation:

$$\%\text{error} = \nabla I_O / I_{\rm O\,match.}\% = \nabla K_1 / 2K_1\% \tag{21}$$

Table 1. Aspect ratios of the proposed current-mode multiplier.

Transistor	Aspect ratio W/L [μm/ μm]
M_{1A}, M_{2A}, M_{1B}, M_{2B}, M_{1C}, M_{2C}, M_{1D}, M_{2D}.	4/6
M_{3A}, M_{4A}, M_{3B}, M_{4B}, M_{3C}, M_{4C}, M_{3D}, M_{4D}.	14/12
M_5, M_6.	90/4
M_7, M_8.	180/4

Table 2. Aspect ratios of the BOTA driving circuit.

Transistor	Aspect ratio W/L [μm/ μm]
M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{20}.	2/3
M_{21}, M_{22}, M_{23}, M_{24}, M_{25}, M_{26}.	20/2

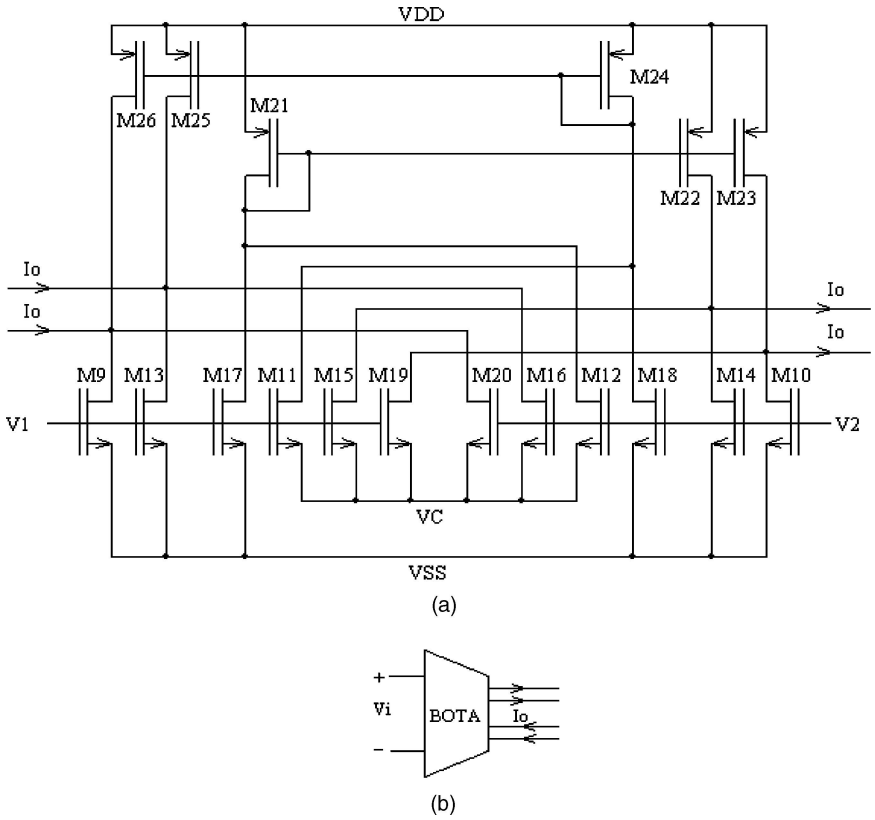

Fig. 3. (a): CMOS realization of the balanced output transconductor (BOTA) [1], (b): Symbol of the balanced output transconductor (BOTA) [1].

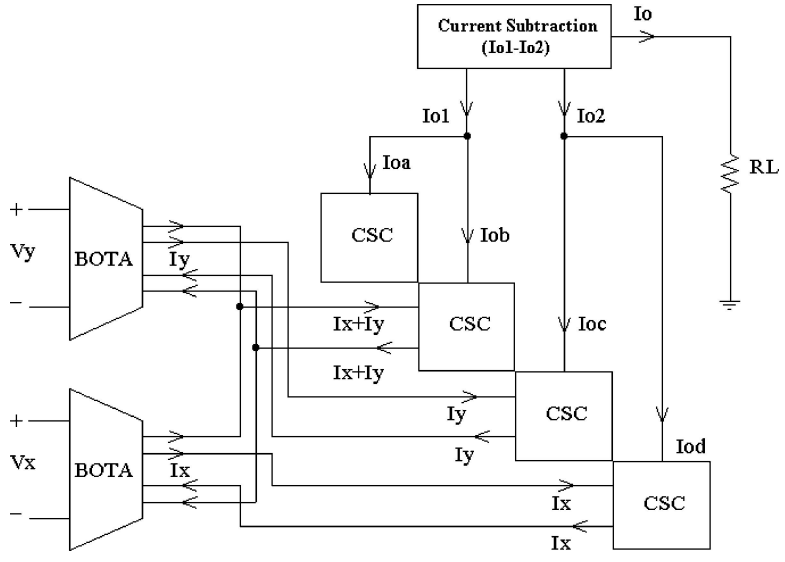

Fig. 4. Block diagram of the proposed voltage-mode multiplier.

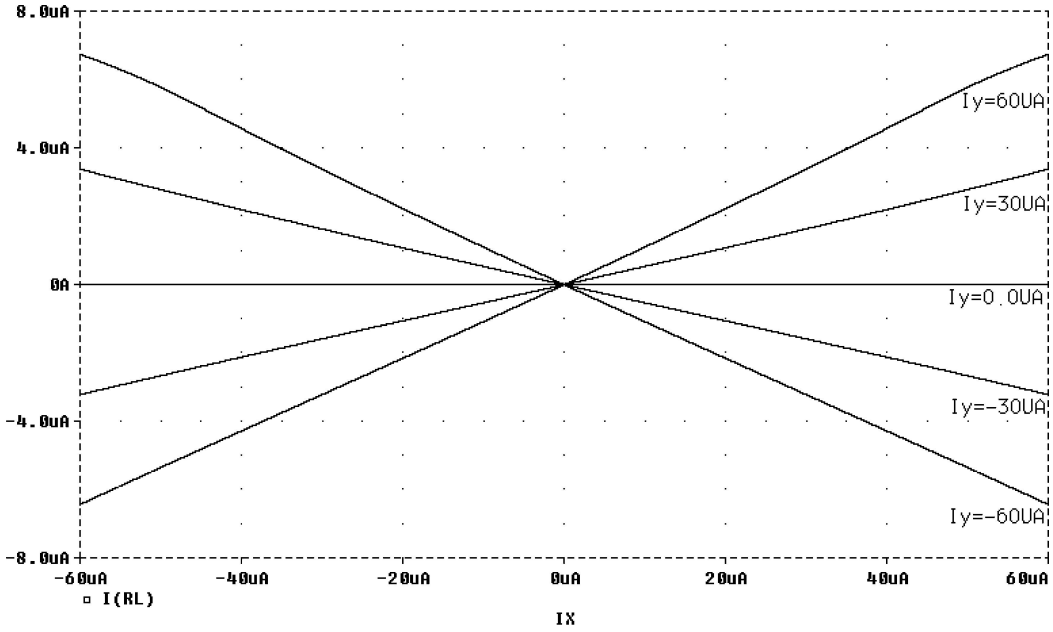

Fig. 5. DC transfer characteristics of the proposed current-mode multiplier of Fig. 2.

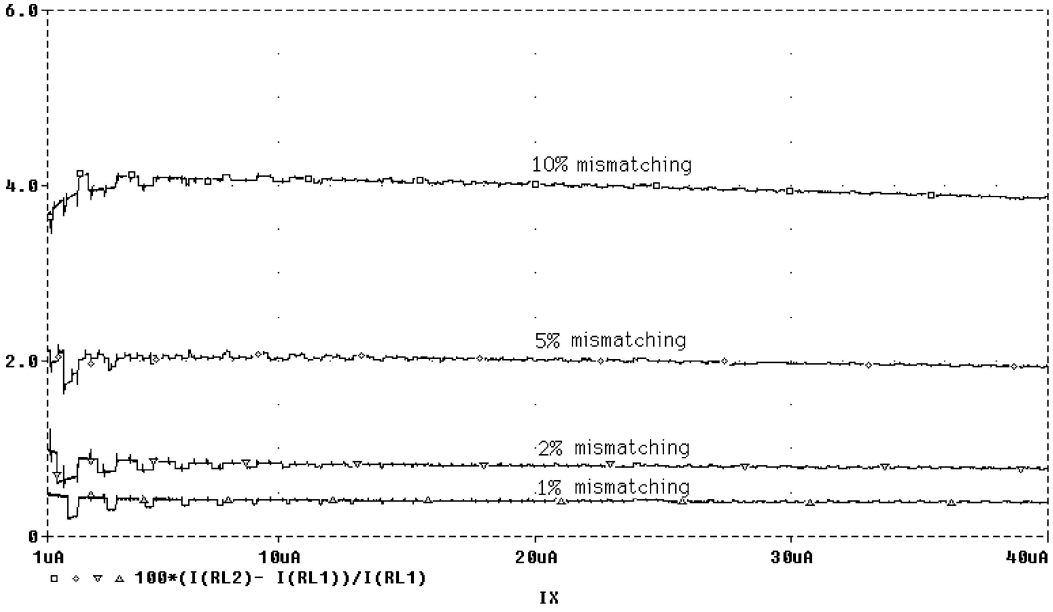

Fig. 6. Percentage error of the output current of the current-mode multiplier due to mismatching effect (at 1, 2, 5 and 10% of mismatching).

3. Four Quadrant CMOS Voltage-Mode Multiplier

The four-quadrant current-mode multiplier discussed in Section 2 not only has simple core and can be designed to have wide input range, but also it can be easily converted to operate in voltage-mode using balanced output transconductor (BOTA) given in [1]. The BOTA circuit is shown in Fig. 3. It is suitable for driving the proposed current-mode multiplier where it has

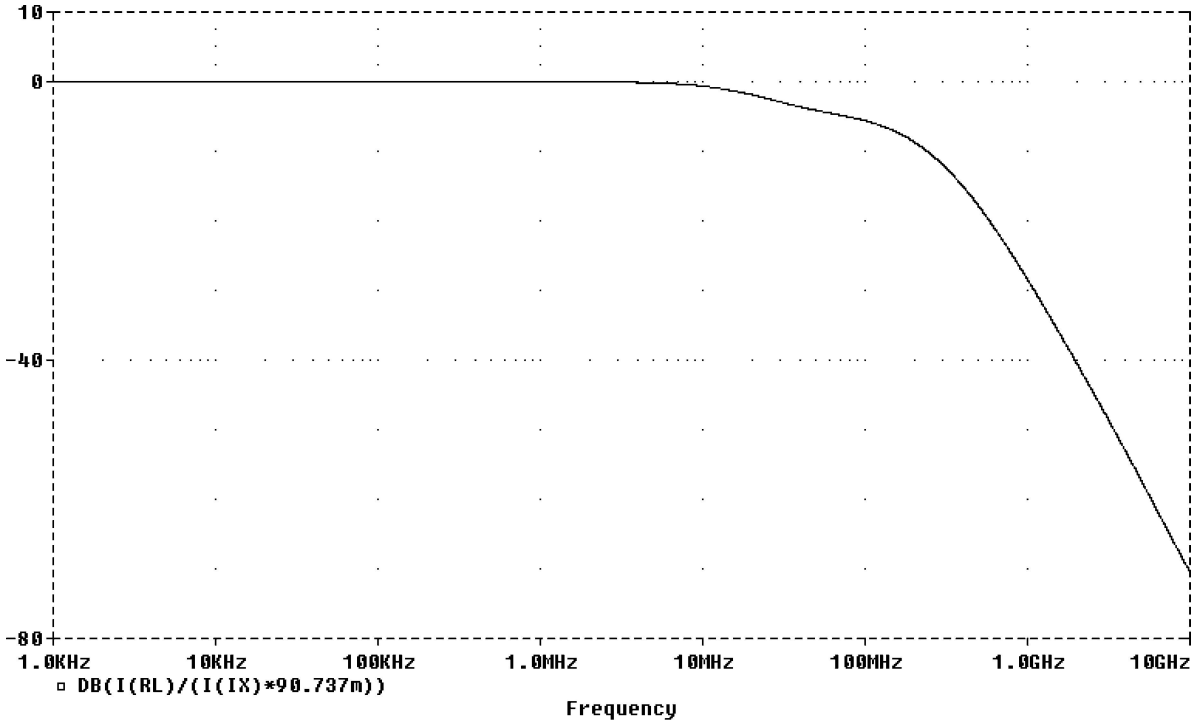

Fig. 7. Normalized frequency characteristics of the proposed current-mode multiplier.

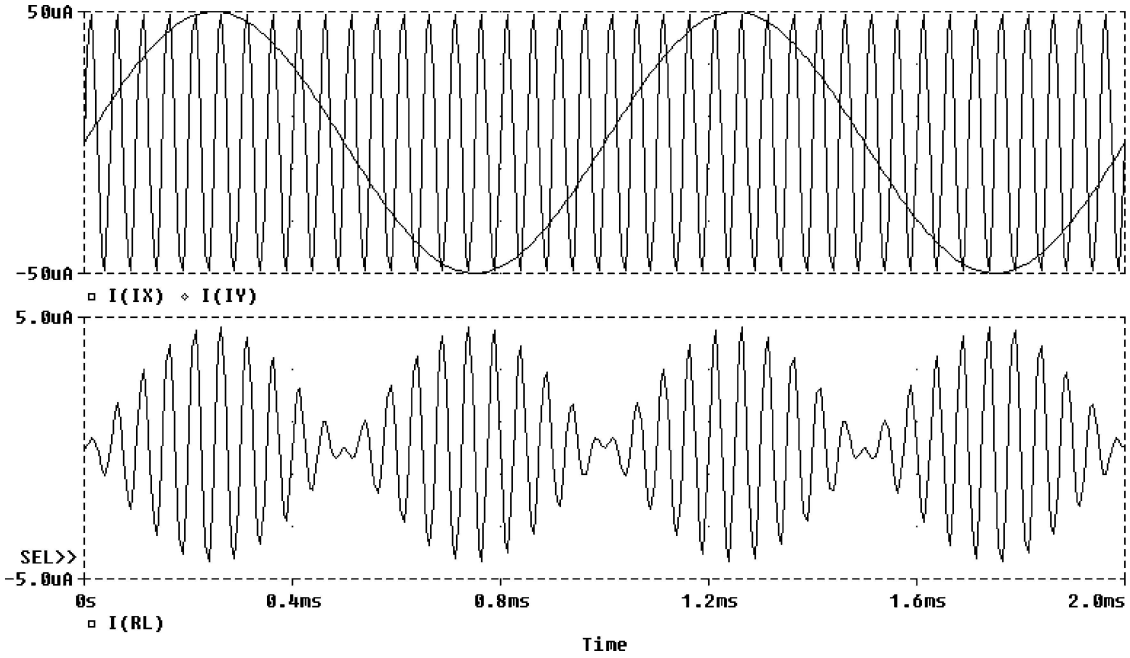

Fig. 8. The current-mode multiplier as an analog amplitude modulator.

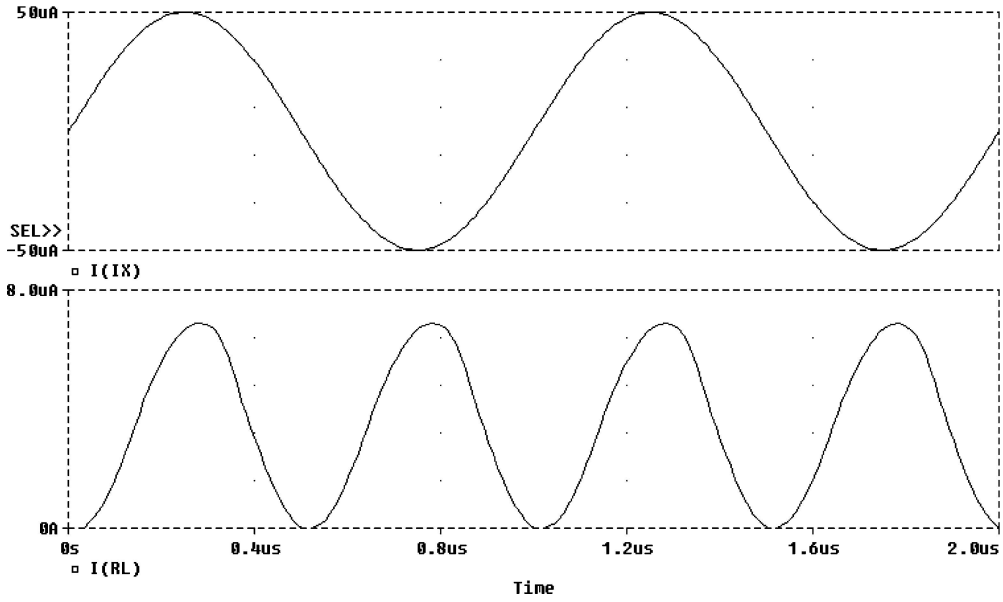

Fig. 9. The current-mode multiplier as a frequency doubler.

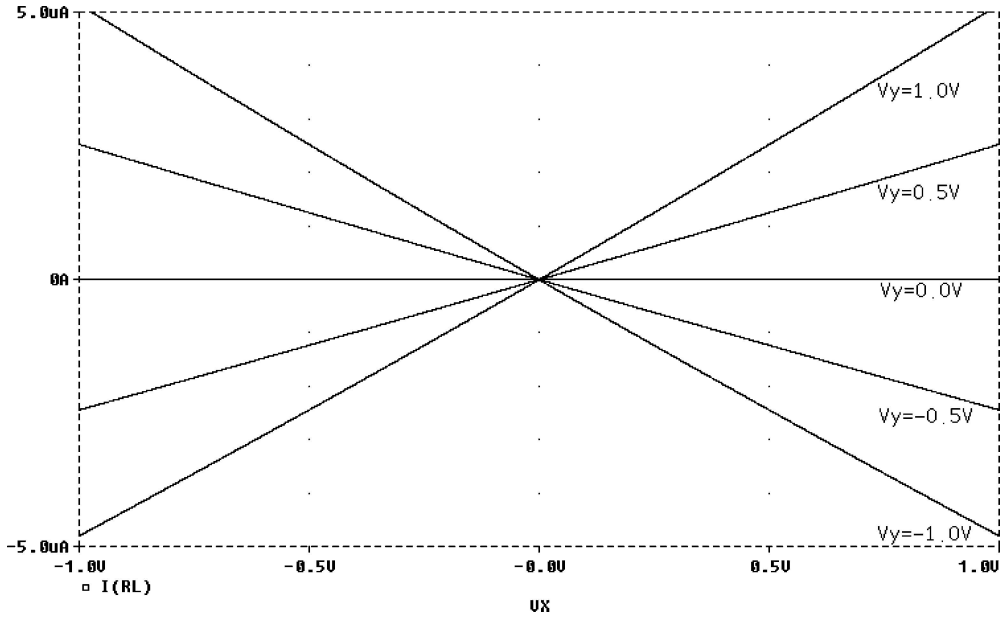

Fig. 10. DC transfer characteristic of the proposed voltage-mode multiplier of Fig. 4.

two balanced output currents as shown in Fig. 3(a). The BOTA operates as a balanced output transconductor with a programmable transconductance G that controlled by the control voltage V_C and is given by:

$$G = K_9(V_C - V_{SS}) \tag{22}$$

And the output current of the BOTA is given by:

$$I_O = G(V_1 - V_2) = K_9(V_C - V_{SS})(V_1 - V_2) \tag{23}$$

Where, K_9 is transconductance parameter of transistors M_9 to M_{20}, and $(V_1 - V_2)$ is the differential input

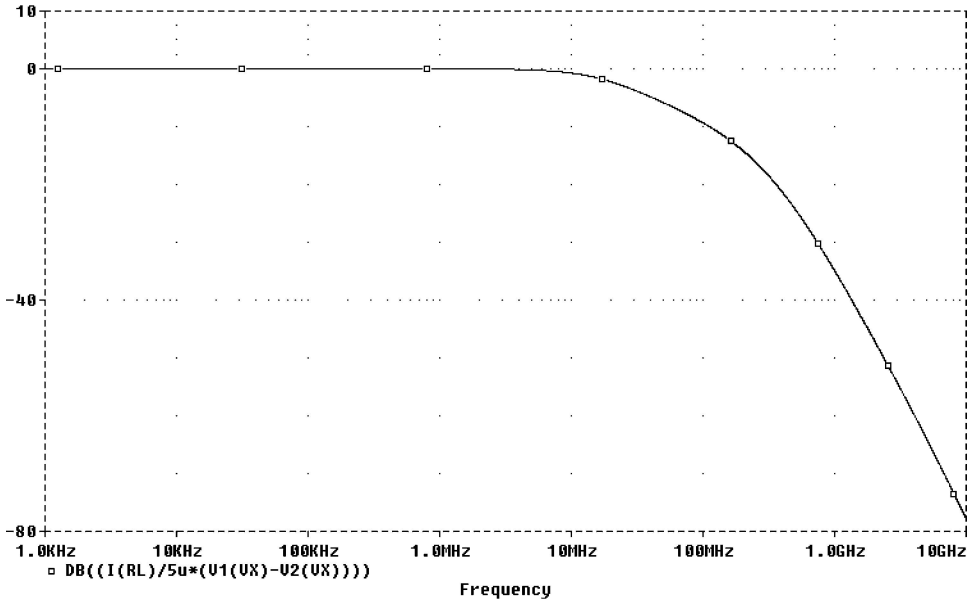

Fig. 11. Normalized frequency characteristics of the proposed voltage-mode multiplier.

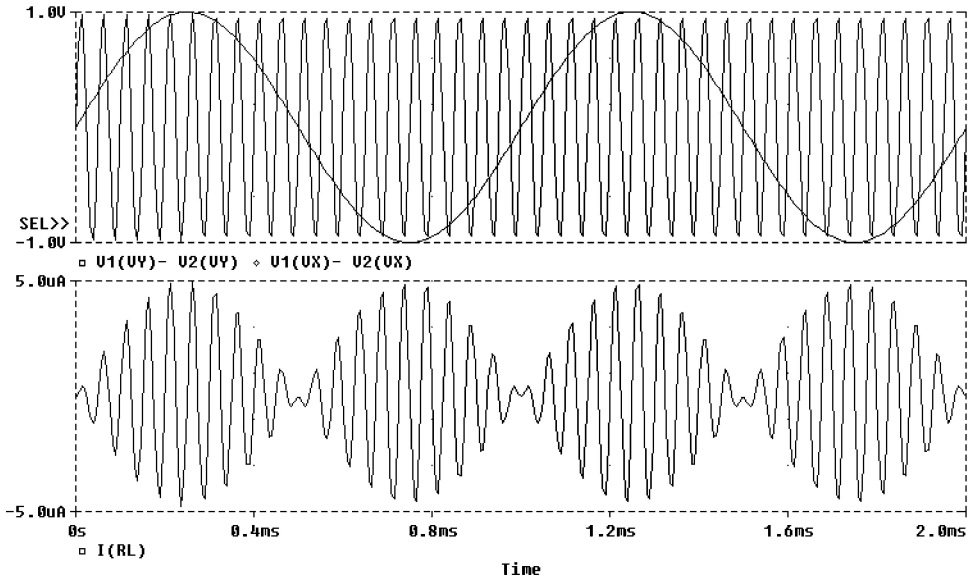

Fig. 12. The voltage-mode multiplier as an analog amplitude modulator.

voltage of the BOTA respectively. The symbol of the used BOTA is shown in Fig. 3(b).

The complete block diagram of the proposed four-quadrant voltage-mode multiplier is shown in Fig. 4. It is consist of the current-mode multiplier of Fig. 2 driven by two BOTA circuits of Fig. 3.

Assuming that V_X and V_Y are the two differential input voltages of the two BOTAs; the overall output current of the multiplier can be deduced using equations (15) and (23) as follow:

$$I_O = 2K_1R^2(K_9(V_C - V_{SS}))^2V_XV_Y \qquad (24)$$

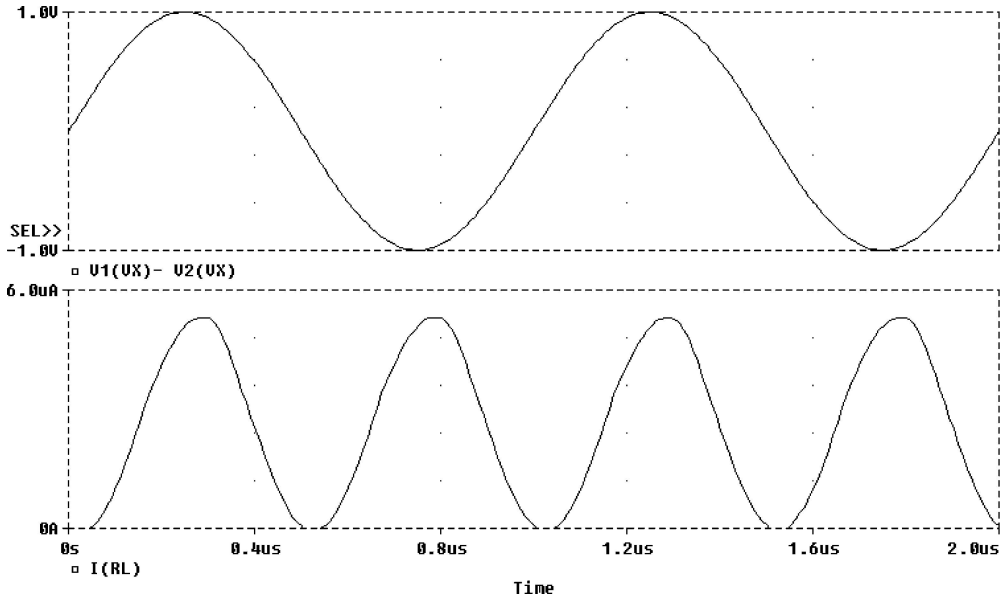

Fig. 13. The voltage-mode multiplier as a frequency doubler.

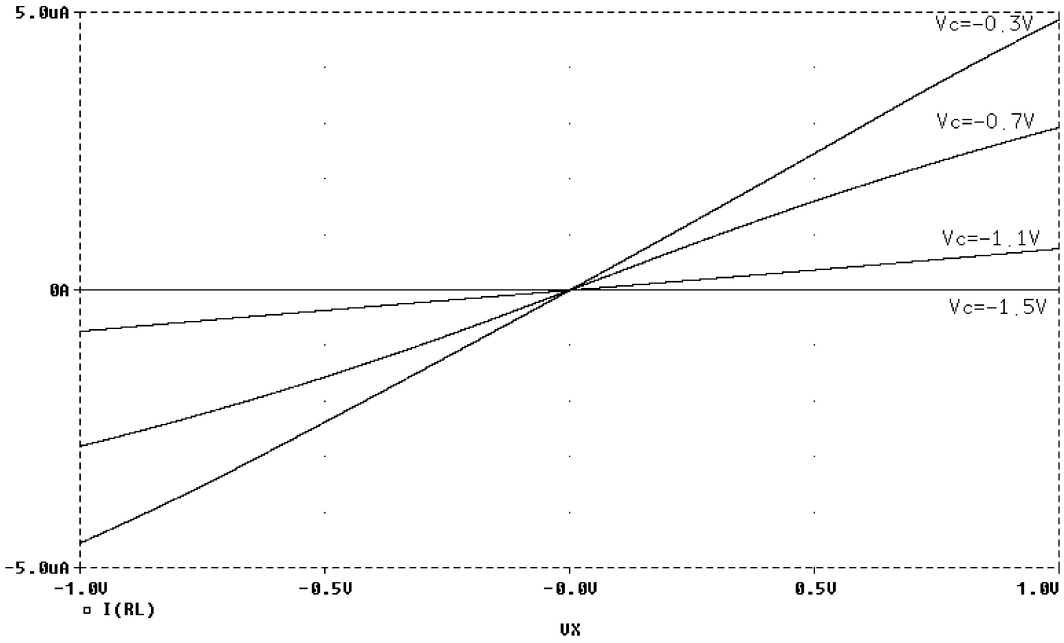

Fig. 14. DC transfer characteristics of the proposed voltage-mode multiplier with V_C as a parameter and $V_Y = 1$ V.

Equation (24) yields the voltage multiplication of the differential input voltages V_X and V_Y. The overall multiplier gain is $(2K_1R^2(K_9(V_C - V_{SS}))^2)$ which is controlled by the control voltage V_C of the BOTA circuit.

4. Simulation Results

Simulation results are given in this section using PSPICE with 0.5 μm CMOS parameters. The power

Table 3. Summary of the simulated results of the proposed multipliers.

	Proposed current-mode multiplier	Current-mode multiplier presented in [7]
Supply voltage	±1.5 V	+5 V
Input range	±60 μA	±20 μA
Static power consumption (@ $Ix = Iy = 0$ μA)	0.671 mW	0.8 mW
Maximum power consumption (Proposed: @ $Ix = Iy = 60$ μA) ([7]: @ $Ix = Iy = 60$ μA)	0.72 mW	0.93 mW
Bandwidth	31 MHz	25.34 MHz
Input referred noise current	0.046 $nA/\sqrt{\text{Hz}}$	27.4 $nA/\sqrt{\text{Hz}}$
Maximum linearity error(Proposed: @ $I_x = I_y = 50$ μA) ([7]: @ $I_x = I_y = 20$ μA)	3.9%	1.22%
%THD (Proposed: @ $I_y = 50$ μA, $I_x = 50\sin(2\pi f_x)\mu$A, $f_x = 1$ MHz) ([7]: @ $Iy = 20$ μA, $Ix = 20\sin(2\pi f_x)\mu$A, $f_x = 1$ MHz)	4.485%	1.54%

Table 4. Simulation results of the proposed voltage multiplier as compared with the results of [2].

	Proposed voltage-Mode multiplier	Voltage-mode multiplier Presented in [2]
Supply voltage	±1.5 V	±1.5 V
Input range	±1 V	0.5±1 V
Bandwidth	25.34 MHz	≈ 30 MHz
Input referred noise voltage	0.85 $\mu\text{V}/\sqrt{\text{Hz}}$	
Static power consumption (Proposed: @ $V_X = V_Y = 0$ V)	1.6 mW	
Maximum power consumption (Proposed: @ $V_X = V_Y = 1$ V)	1.85 mW	
%THD (Proposed: @$V_Y = 1$ V, $V_X = 1\sin(2\pi f_x)$V, $f_x = 1$ MHz) ([2]: @Vy0=1.5 V, Vy1= −0.5 V, Vx1= −0.5 V Vx0 = 1 $\sin(2\pi f_x)$V, $f_{x0} = 1$ MHz)	4.667%	4.4%

supply voltages V_{DD} and V_{SS} are balanced (1.5 V and −1.5 V) respectively.

Figure 5 shows the DC transfer characteristic of the four-quadrant current-mode multiplier of Fig. 2. The aspect ratios of the transistors are given in Table 1, $V_G = 3$ V and the load resistance R_L is equal to 10 KΩ.

Figure 6 shows the percentage error of the output current of the multiplier due to mismatching between transistors M_1 and M_2 for different values of mismatching, namely, 1, 2, 5, and 10%. I_Y is set to 40 μA and I_X is swept from 0 to 40 μA.

Figure 7 shows the normalized frequency characteristic of the multiplier. Where, I_Y is set to 50 μA DC and I_X is the AC-varying signal with 50 μA magnitude. The −3 dB bandwidth and the input referred noise current of the multiplier are 31 MHz and 46 pA/$\sqrt{\text{Hz}}$, respectively.

Figure 8 demonstrates the use of the multiplier as an analog amplitude modulator where I_X is the sinusoidal modulating signal with magnitude equal to 50 μA and frequency ($f_x = 1$ KHz) while I_Y is the sinusoidal carrier with amplitude equal to 50 μA and frequency ($f_y = 20$ KHz).

Figure 9 shows the use of the multiplier as a frequency doubler. Where, $I_X = I_Y = 50\sin(2\pi f_i t)$ μA and $f_i = 1$ MHz.

The DC transfer characteristic of the four-quadrant voltage-mode multiplier of Fig. 4 is shown in Fig. 10. The same aspect ratios of the transistors given in Table 1 are used in addition to aspect ratios given in Table 2, $R_L = 10$ KΩ. It is clear that the voltage-mode multiplier has wide differential-voltage input range with excellent output linearity. The differential-voltage input varies from −1 V to 1 V.

The normalized frequency characteristic of the multiplier is shown in Fig. 11, where, V_Y is set to 1 V DC and V_X is the AC-varying signal with 1 V magnitude. The multiplier has a bandwidth of 25.34 MHz and input referred noise voltage of 0.85 $\mu V/\sqrt{\text{Hz}}$.

Figure 12 shows the use of the multiplier as an analog amplitude modulator. V_X is the sinusoidal modulating signal with magnitude equal to 1 V and frequency (f_x = 1 KHz) while V_Y is the sinusoidal carrier with amplitude equal to 1 V and frequency (f_y = 20 KHz).

Figure 13 shows the use of the multiplier as a frequency doubler. Where, $V_X = V_Y = \sin(2\pi f_i t)$ V and f_i = 1 MHz.

The gain of the voltage-mode multiplier can be controlled using the control voltage of the BOTA (V_C). The DC transfer characteristic of the proposed voltage-mode multiplier is shown in Fig. 14 with V_C as a parameter and V_Y = 1 V.

The simulation results of the proposed four-quadrant current-mode multiplier are summarized and compared with the performance of the current-mode multiplier of [7] in Table 3. Also, the simulation results of the proposed four-quadrant voltage-mode multipliers are summarized and compared with the performance of the voltage-mode multiplier of [2] in Table 4.

5. Conclusion

In this paper, a novel four-quadrant current-mode multiplier based on a novel squarer cell has been proposed. This multiplier has simple core and can be designed to have wide input current range with low power consumption, moreover it can be easily converted to voltage-mode by using BOTA circuit with wide input voltage range. The proposed circuits were confirmed by using PSPICE simulation and found to have good linearity with wide input dynamic range. The simulations also included the power consumption, the frequency bandwidth, input referred noise, mismatching effect, maximum linearity error, and %THD.

References

1. Mahmoud, S.A. and Soliman, A.M. "CMOS balanced output transconductors for analog VLSI." *Microelectronics Journal*, vol. 30, pp. 29–39, 1999.
2. Suzuki, T., Oura, T., Yoneyama, T., and Asai, H. "Design and simulation of 4Q-multiplier using linear and saturation regions of MOSFET complementally." *IEICE Trans. Fundamentals*, vol. E85-A, pp. 1242–1248, 2002.
3. Han, G. and Sanchez-Sinencio, E. "CMOS transconductance multiplier: A tutorial." *IEEE Trans. Circuit Syst. II*, vol. 45, pp. 1550–1563, 1998.
4. Toumazou, C., Lidgey, J., and Haigh, D. *Analogue IC Design: The Current Mode Approach*. Peregrinus, London, U.K., 1990.
5. Alzaher, H.A., Elwan, H., and Ismail, M. "A CMOS fully balanced second-generation current conveyor." *IEEE Trans. Circuit Syst. II*, vol. 50, pp. 278–287, 2003.
6. Liu, B.D., Hang, C.Y., and Wu, H.Y. "Modular current-mode defuzzification circuit for fuzzy logic controls." *Electronics Lett.*, vol. 30, pp. 1287–1288, 1994.
7. Tanno, K., Ishizuka, O., and Tang, Z. "Four-Quadrant CMOS Current-Mode Multiplier Independent of Device parameters," *IEEE Trans. Circuit Syst. II*, vol. 47, pp. 473–477, 2000.

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