Fully differential CMOS CCII based on differential difference transconductor

Soliman A. Mahmoud

Abstract This paper presents a new CMOS fully differential second-generation current conveyor (FDCCII). The proposed FDCCII is based on a fully differential difference transconductor as an input stage and two class AB output stages. Besides the proposed FDCCII circuit is operating at supply voltages of ± 1.5 V, it has a total standby current of 380 μA. The application of the FDCCII to realize variable gain amplifier, fully differential integrator, and fully differential second order bandpass filter are given. The proposed FDCII and its applications are simulated using CMOS 0.35 μm technology.

Keywords Current conveyor · Fully differential current conveyor · Bandpass filter · Variable gain amplifier

1 Introduction

Analog circuit design using the current mode approach has recently gained considerable attention. This stems from its inherent advantages of wide bandwidth, high slew rate low power consumption and simple circuitry [1]. The second generation current conveyor (CCII) is one of the most versatile current mode building bocks. Since its introduction [2], it has been used in a wide range of applications and several circuit realizations have been proposed for its implementation [e.g., 3–8]. The CCII is a single ended device; however, most modern high performance analog integrated circuits incorporate fully differential signal paths. This is because fully differential circuit configurations have been widely used in high-frequency analog signal applications like switched capacitor filters [9] and mute-standard wireless receivers [10]. As compared to their single ended counterparts, they have higher rejection capabilities to clock-feed-through, charge injection errors and power supply noises, larger output dynamic range, higher design flexibility, and reduced harmonic distortion. Moreover, most modern systems employ both analog and digital parts on the same chip. A fully differential architecture of the analog part becomes more essential as it provides immunity to digital noise.

In this paper, a new fully differential CMOS second-generation current conveyor (FDCCII) is proposed. The proposed CMOS realization of the FDCCII is based on a new fully differential difference transconuctor as an input stage and two class AB output stages. The FDCCII has the advantages of the single ended CCII beside the advantages of the fully differential signal processing. The FDCCII has many useful applications like the single ended CCII [1]. The FD-CCII is basically a fully differential device as shown in Fig. 1. The Y_1 and Y_2 terminals are high impedance terminals while X_1 and X_2 terminals are low impedance ones. The differential input voltage V_{Y12} applied across Y_1 and Y_2 terminals is conveyed to a differential voltage V_{X12}; i.e., ($V_{X12} = V_{Y12}$). The input currents applied to the X_1 and X_2 terminals are conveyed to the Z_1 and Z_2 terminals, i.e. ($I_{z1} = I_{x1}$ and $I_{z2} = I_{x2}$). The Z_1 and Z_2 terminals are high impedance nodes suitable for current outputs.

The paper is organized as the follow, in Section 2, the realization of the FDCCII is presented. In Section 3, the applications of the FDCCII in realizing fully differential integrator, fully differential second order bandpass filter with independent gain-bandwidth and a high quality factor are given. PSpice simulations of the proposed FDCCII and its applications using CMOS 0.35 μm technology are also given.

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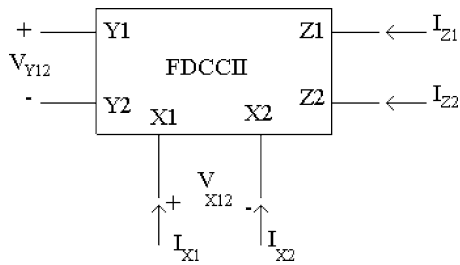e-mail: amahmoud@frcu.eun.eg

Fig. 1 The symbol of the FDCCII

2 CMOS realization of the FDCCII

The overall CMOS circuit of the FDCII is shown in Fig. 2. The proposed FDCCII is consisting of a differential difference transconductor formed from transistors $M1$ to $M16$, current mirror formed from $M17$ to $M21$ and $M37$ to $M39$, two class AB output stages ($M25$ to $M30$) and ($M31$ to $M36$) and the biasing of the output stages ($M22$ to $M24$). All transistors are assumed to be operating in the saturation.

Transistors $M1$ to $M8$ are assumed to be matched transistors with transconductance parameter K, and their currents are linearized by using the four biasing circuits formed from $M9$ to $M16$. First, expressions for the biasing voltages V_a, V_b. V_c, V_d in terms of V_1, V_2, V_3, V_4, respectively, are obtained. Consider the biasing circuit formed from $M11$ and $M15$; the current flowing through $M11$ is given by:

$$I_{11} = \frac{K_{11}}{2}(V_{Y2} - V_a - V_T)^2 \tag{1}$$

Where ($K_{11} = \mu_n C_{ox} \{\frac{W}{L}\}_{11}$) is the transconductance parameter of transistor $M11$, μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area and $\{\frac{W}{L}\}_{11}$ is the aspect ratio.

And the same current flowing through $M15$ is given by:

$$I_{15} = \frac{K_{15}}{2}(V_B - V_{SS} - V_T)^2 \tag{2}$$

Where V_B is the control voltage, taking $K_{11} = K_{15}$; hence from Eqs. (1) and (2), the biasing voltage V_a is given by:

$$V_a = V_{Y2} - V_B + V_{SS} \tag{3}$$

Similar expression for the biasing voltages V_b, V_c, V_d can be obtained and are given, respectively, by:

$$V_b = V_{Y1} - V_B + V_{SS} \tag{4}$$

$$V_c = V_{X2} - V_B + V_{SS} \tag{5}$$

$$V_d = V_{X1} - V_B + V_{SS} \tag{6}$$

Therefore, the currents through $M1$ to $M8$ can be obtained. The currents through $M1$ to $M4$ can be written as:

$$I_1 = \frac{K}{2}(V_{Y2} - V_{SS} - V_T)^2 \tag{7}$$

$$I_2 = \frac{K}{2}(V_{Y1} - V_{SS} - V_T)^2 \tag{8}$$

$$I_3 = \frac{K}{2}(V_{X2} - V_{SS} - V_T)^2 \tag{9}$$
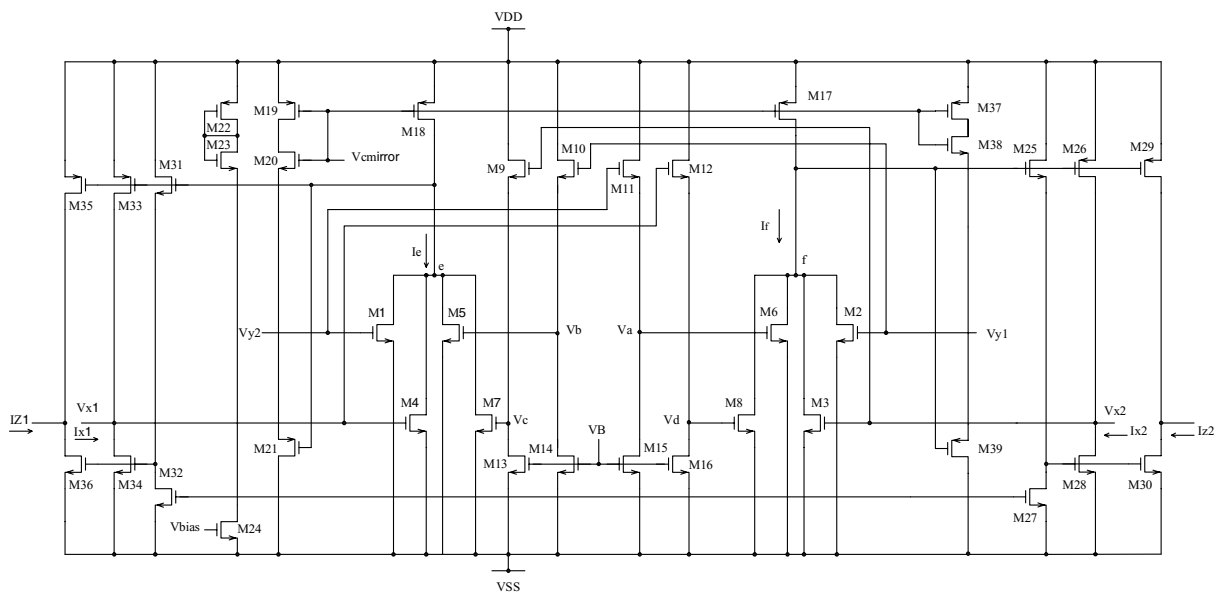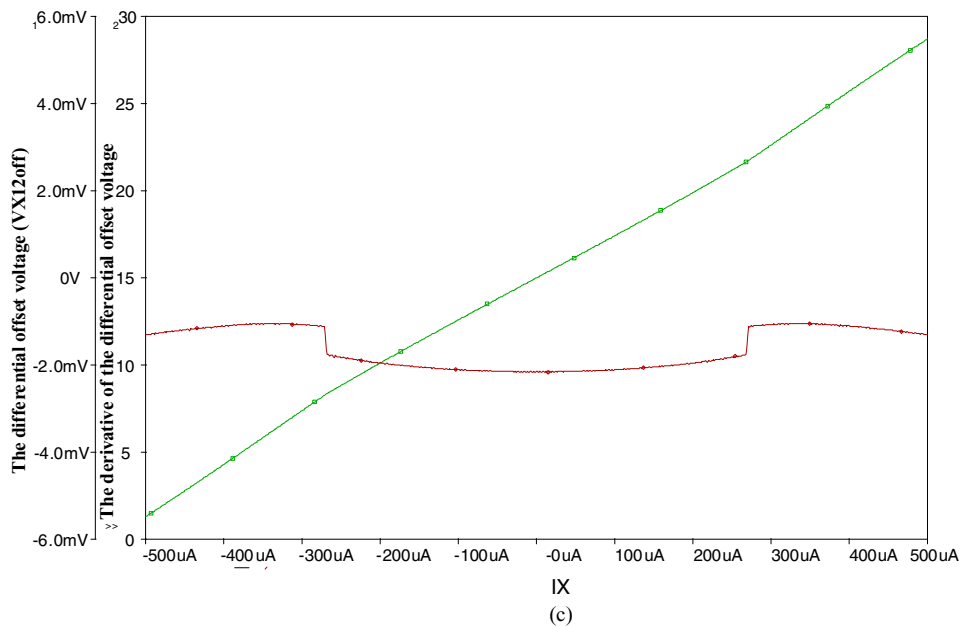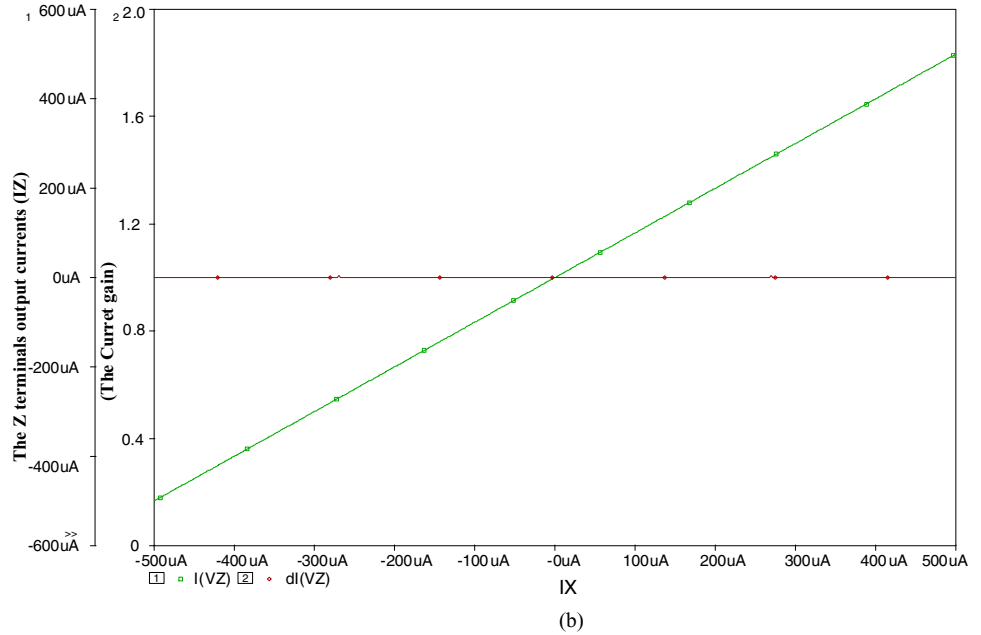
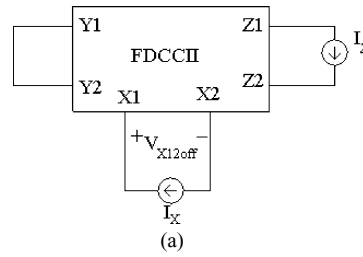$$I_4 = \frac{K}{2}(V_{X1} - V_{SS} - V_T)^2 \tag{10}$$

Fig. 2 The CMOS circuit of the FDCCII

Fig. 3 (a) FDCCII as a current buffer, (b) The variations of the output current I_Z and its transfer gain with respect to the input current I_X. For the FDCCII shown in Fig. 2(a) and (c) The differential offset voltage across the $X1$ and $X2$ terminals along its derivative for the FDCCII shown in Fig. 2(a)

The currents of transistors $M5$ to $M8$ are given by:

$$I_5 = \frac{K}{2}(V_{Y1} - V_B - V_T)^2 \tag{11}$$

$$I_6 = \frac{K}{2}(V_{Y2} - V_B - V_T)^2 \tag{12}$$

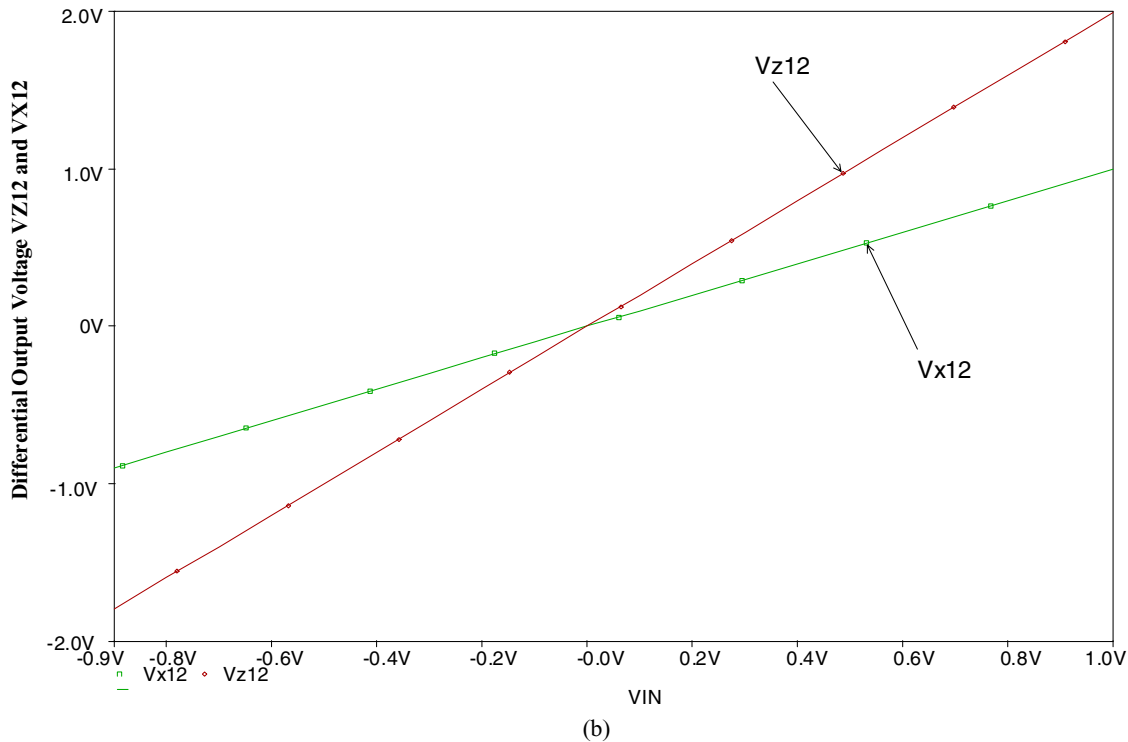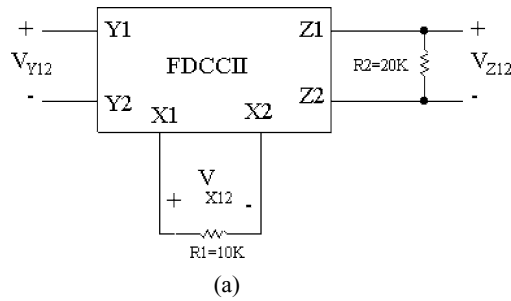$$I_7 = \frac{K}{2}(V_{X2} - V_B - V_T)^2 \tag{13}$$

Fig. 4 (a) The FDCCII based amplifier of Gain $= 2$, and (b) The voltage swings V_{X12} and V_{Z12} of the FDCII based amplifier shown in Fig. 4(a)

$$I_8 = \frac{K}{2}(V_{X1} - V_B - V_T)^2 \tag{14}$$

The output current of the input stage transconductor I_{out} is defined as:

$$I_{out} = I_f - I_e \tag{15}$$

From Fig. 1

$$I_{out} = (I_2 + I_3 + I_6 + I_8) - (I_1 + I_4 + I_5 + I_7) \tag{16}$$

By substituting from Eqs. (7) to (14) in Eq. (16), the transcondutor output current is given by:

$$I_{out} = G_m[(V_{y1} - V_{y2}) - (V_{x1} - V_{x2})] \tag{17}$$

Where

$$G_m = K(V_B - V_{SS}) \tag{18}$$

By the current mirror action of transistors $M17$, $M18$ and $M19$, the current I_f forced to be equal I_e (i.e. $I_{out} = I_f - I_e = 0$). Therefore from Eq. (17):

$$V_{y1} - V_{y2} = V_{x1} - V_{x2} \tag{19}$$

In order to minimize the voltage offset between the X and Y terminals, V_e must be small and very close to V_f, which is approximately equal to zero for low values of the X-terminal currents.

For proper operation of the current mirror, the bias voltage $V_{cmirror}$ must be adjusted to make V_e equal to zero as

follows:

$$V_{c\,\text{mirror}} = \frac{\sqrt{K_{19}}(V_{DD} - |V_{Tp}|) + \sqrt{K_{\text{eff}}}(V_{Tn} + |V_{Tp}|)}{\sqrt{K_{19}} + \sqrt{K_{\text{eff}}}}$$

$$(20)$$

Where

$$K_{\text{eff}} = \frac{\sqrt{K_{20}K_{21}}}{\sqrt{K_{20}} + \sqrt{K_{21}}} \qquad (21)$$

The expression of the $V_{c\text{mirror}}$ can be obtained simply as follow, transistors M_{20}, M_{21} work as a composite transistor with effective transconductance parameter K_{eff} given in Eq. (21), therefore the current through M_{20}, M_{21} is given by:

$$I_{20} = I_{21} = \frac{K_{\text{eff}}}{2}(V_{c\,\text{mirror}} - V_e - V_{Tn} - |V_{Tp}|)^2 \qquad (22)$$

Transistor M_{19} act as a current source and this current is given by:

$$I_{19} = \frac{K_{19}}{2}(V_{DD} - V_{c\,\text{mirror}} - |V_{Tp}|)^2 \qquad (23)$$

But the current flowing through $M19$ is the same as that of M_{20}, M_{21}. Therefore the bias voltage $V_{c\,\text{mirror}}$ to make V_e equal to zero is given in Eq. (20).

To maintain a good current drive capability with low output impedance outputs, class AB output stages are used. Transistors ($M26$, $M28$) and ($M33$, $M34$) form the push pull output stage transistors. The level shift circuits formed by ($M25$, $M27$) and ($M31$, $M32$) are used to realize controlled

(a)

(b)
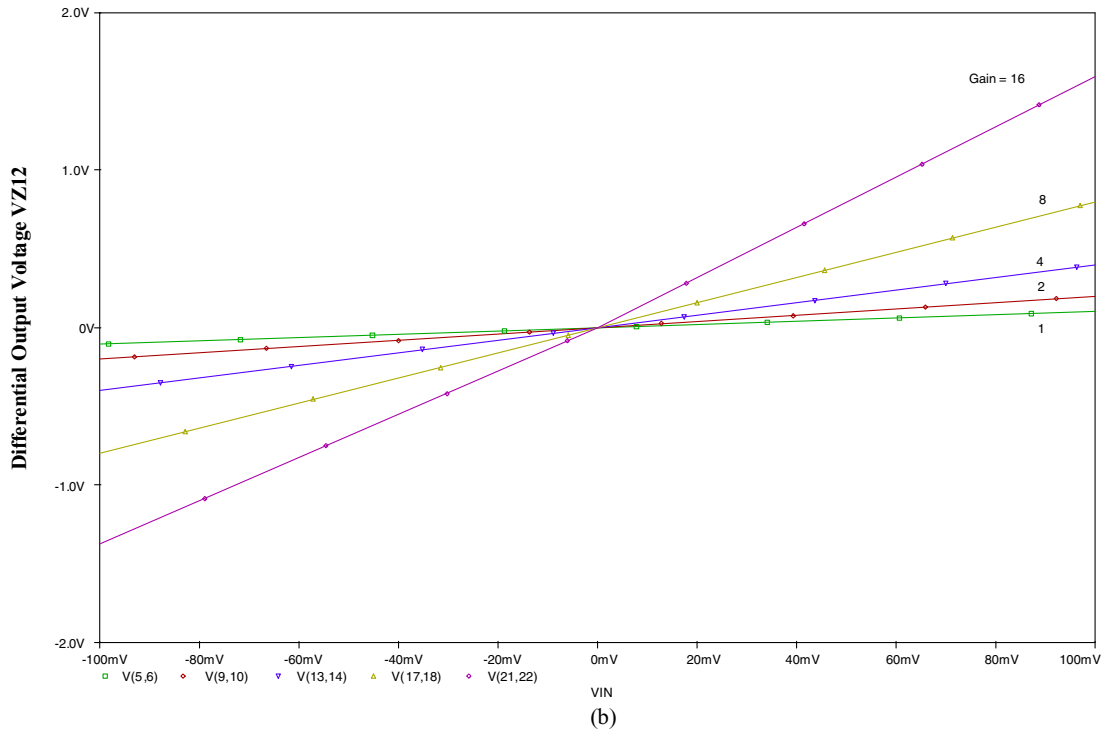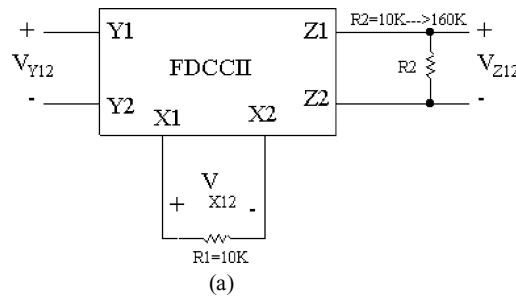
Fig. 5 (a) The FDCCII based variable gain amplifier, (b) The DC transfer characteristic of the FDCCII based Variable Gain Amplifier (VGA) for different values of $R2$, (c) The frequency response of the FDCCII based Variable Gain Amplifier (VGA), and (d) The input and output refereed noise spectral densities
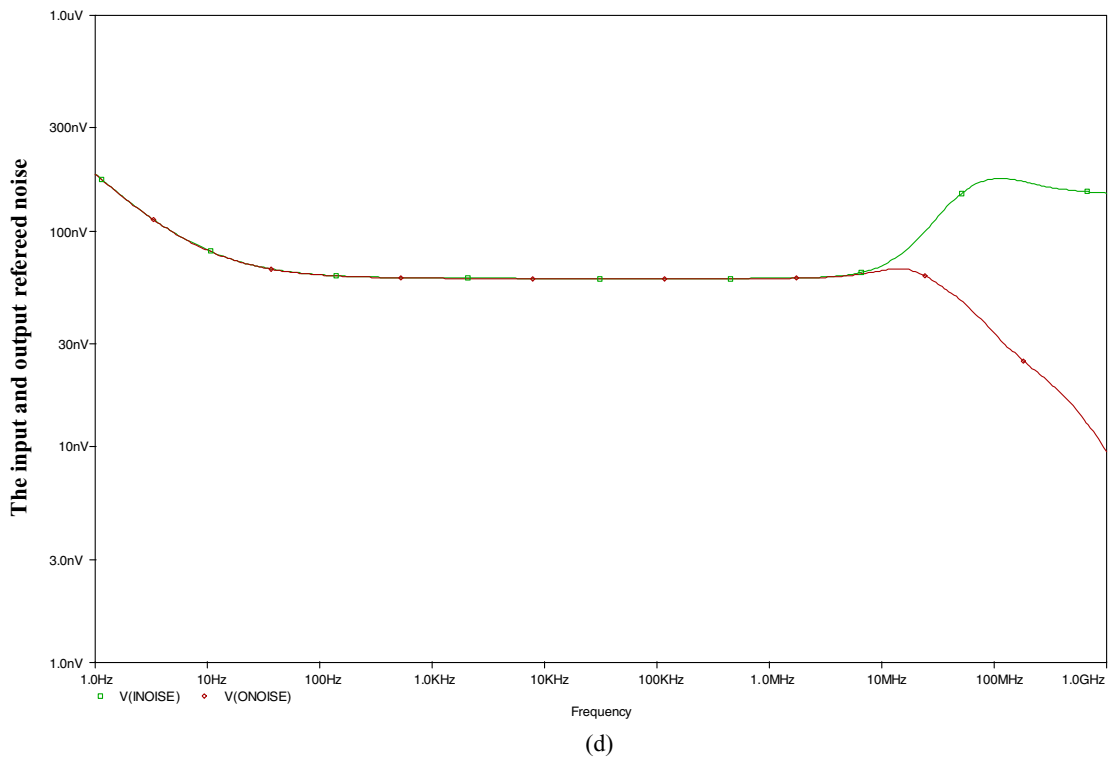
(c)

(d)
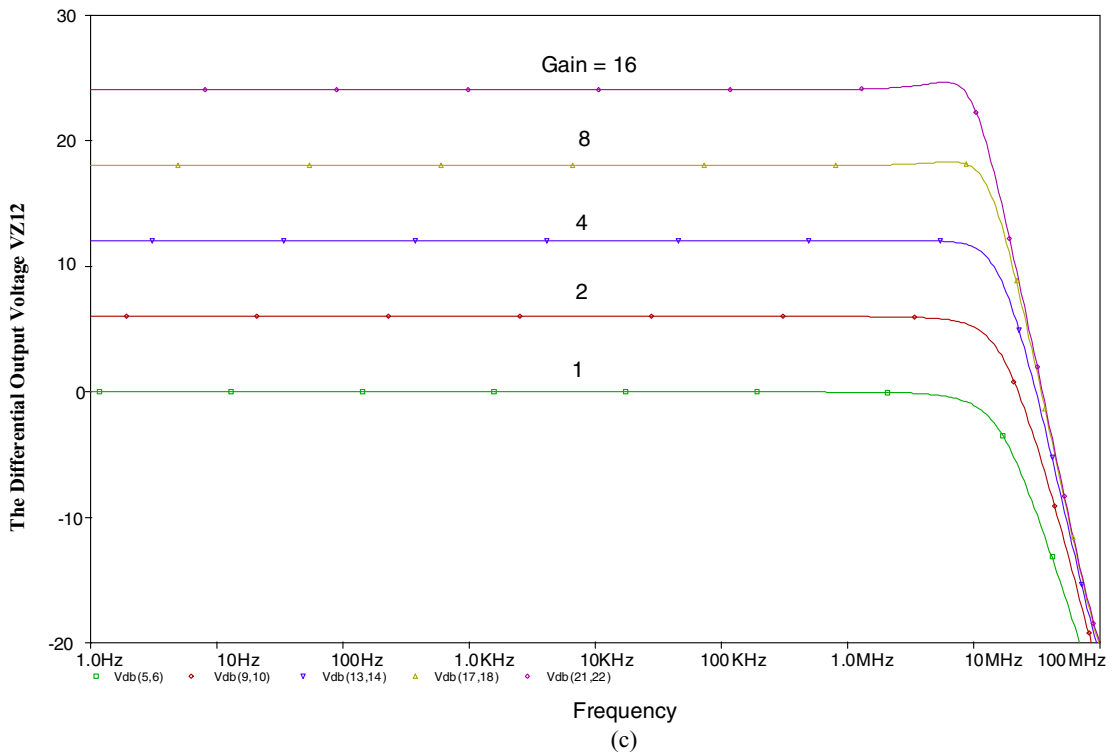
Fig. 5 (Continued)

floating voltage sources that controls the standby current through the output stage transistors. The standby current is adjusted by the biasing circuit formed of $M22$, $M23$ and $M24$. The standby power consumption of the output stages for the dual power supply is given by:

$$P_{SB} = 2V_{DD}(3I_{SB} + K_{25}(V_{DD} - V_{Tn} + V_{Tp})^2) \qquad (24)$$

The last term in the above equation is the current through the level shift transistors ($M25$, $M27$) and ($M31$, $M32$). This current can be kept small by choosing a small aspect ratio
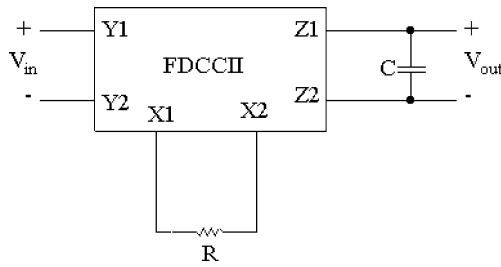
Fig. 6 The FDCCII based fully differential integrator

for ($M25$, $M27$) and ($M31$, $M32$). The class AB output stage enables the circuit to derive heavy resistive and capacitive load with low standby power consumption and no slewing. It is worth mentioning that smaller Miller compensation capacitors can be connected between the gate and drain of transistors $M26$ and $M33$ to ensure good transient response under all load conditions.

The input currents applied to the $X1$ and $X2$ terminals are conveyed to the $Z1$ and $Z2$ terminals by using the transistors ($M35$, $M36$) and ($M29$, $M30$) respectively.

The performance of the proposed FDCCII circuit was verified by performing Pspice simulations with supply voltages ± 1.5 V and using 0.35 μm CMOS technology parameters with transistors aspect ratios as given in Table 1.

Figure 3(b) shows the floating output current across the $Z1$ and $Z2$ terminals when a floating input current I_X is connected across the $X1$ and $X2$ terminals and scanned from -500 μA to 500 μA while the differential voltage across $Y1$ and $Y2$ is set to zero as shown in Fig. 3(a). It has been found that the magnitude of I_Z follows that of I_X with a maximum output

Table 1 Transistors aspect ratios for circuit shown in Fig. 2

Transistors	W (μm)	L (μm)
M_1–M_8	0.7	5.6
M_8–M_{16}	0.7	0.7
M_{17}–M_{19} , M_{37}	14	0.7
M_{20}, M_{38}	17.5	0.7
M_{21}, M_{39}	35	0.7
M_{22}, M_{26}, M_{29}, M_{33}, M_{35}	70	0.7
M_{23}, M_{28}, M_{30}, M_{34}, M_{36}	35	0.7
M_{24}	14	0.7
M_{25}, M_{27}, M_{31}, M_{32}	1.4	0.7

current of 5 mA with a gain error of 0.03% for a 2 mA output current. Figure 3(c) shows the variations of the offset voltage across the $X1$ and $X2$ terminals versus the variation in the input current applied across $X1$ and $X2$ (I_X) when the V_{Y12} is equal to zero. The differential X input resistance (R_{X12}) is less than 15 Ω. The offset voltage is less than 7 mV at $I_z = 500$ μA. Figure 4(b) shows the voltage swings V_{X12} and V_{Z12} when the FDCCII is used to realize a voltage amplifier with gain of two as shown in Fig. 4(a). The DC linearity error is found to be less than 0.01% for a 0.75 V differential input and the maximum differential output voltage is 2.4 V. The power supply rejection ratio (PSRR) from positive supply to the output is 98 dB and from negative supply is 90 dB. The differential DC characteristic of the FDCCII based variable gain amplifier (VGA) shown in Fig. 5(a) of gain 1, 2, 4, 8, 16 is shown in Fig. 5(b). Also, the frequency response of the FDCCII based variable gain amplifier is shown in Fig. 5(c).
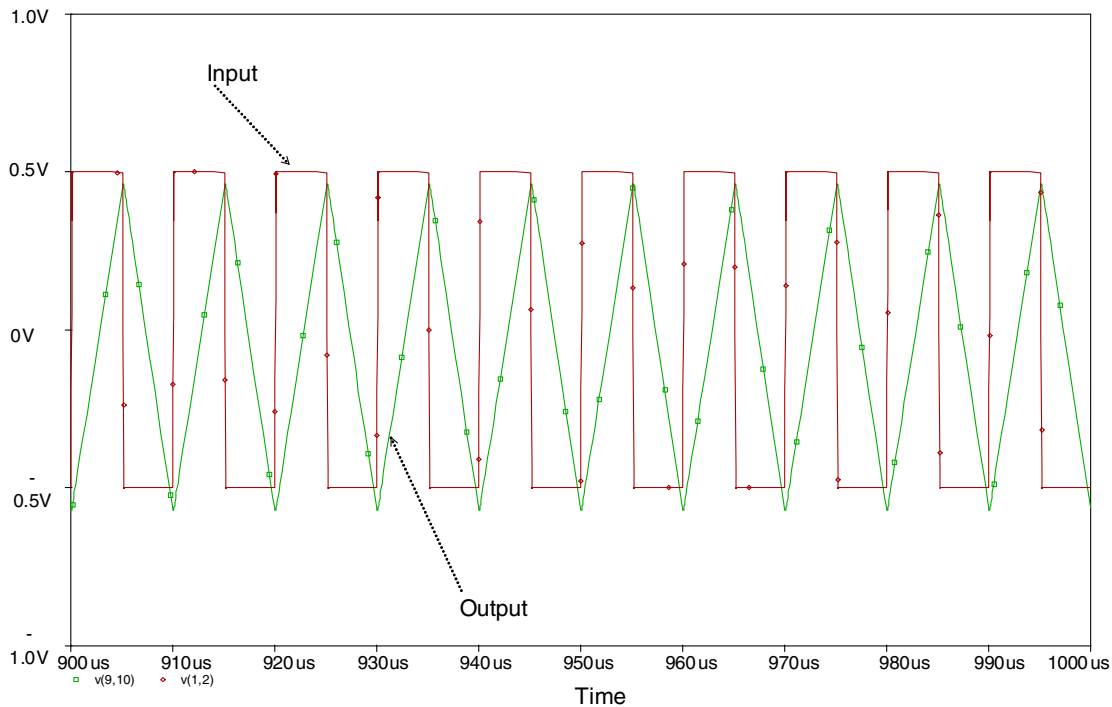
Fig. 7 The output of the integrator along with the square wave input
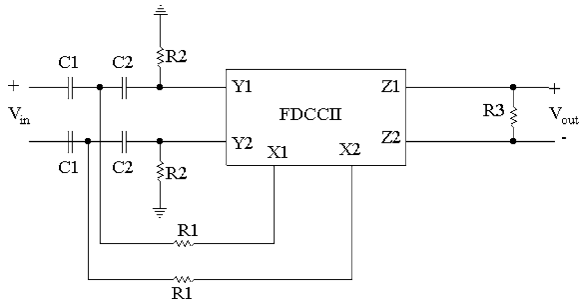
Fig. 8 Fully differential bandpass filter based on the proposed FDCCII

It is clear from Fig. 5(c) that the VGA based on the FDCFOA experiences no loss in bandwidth (which is approximately equal to 26 MHz) when the gain is increased. The input and output voltage noise spectral density is shown in Fig. 5(d) of the FDCCII based unity gain amplifier.

3 Applications

The proposed FDCCII can be used to implement the fully differential or fully balanced architecture of any CCII based circuits. Two design examples are presented in this section to demonstrate the use of the proposed FDCCII.

3.1 Fully differential integrator

The fully differential integrator is a basic building block in realizing continuous time filters [11, 12]. Figure 6 shows the FDCCII based fully differential integrator. The output voltage of the integrator is taken across the buffered Z_1 and Z_2 terminals and is given by:

$$V_{out} = \frac{1}{SCR} V_{in} \qquad (25)$$

PSpice simulations results for the FDCCII based fully differential integrator are shown in Fig. 7 with a square wave input of 1 V peak to peak amplitude and a frequency of 100 KHz, where $R = 10$ KΩ and $C = 250$ pF.

3.2 FDCFOA-based bandpass filter

The FDCCII is used to implement a fully differential version of the Sallen-Key bandpass filter. The filter shown in Fig. 8 represents a filter circuit that realizes second order fully differential bandpass filter based on a single FDCCII. By direct analysis, the following transfer function is obtained as:

$$\frac{V_O}{V_I} = \frac{-\frac{R_3}{R_1 R_2 C_1} S}{S^2 + \frac{S}{R_2}\left[\frac{(C_1+C_2)}{C_1 C_2}\right] + \frac{1}{R_1 R_2 C_1 C_2}} \qquad (26)$$

from the above equation, for equal C design, the ω_o, Q and the gain H of the filter are given by:

$$\omega_O = \frac{1}{\sqrt{R_1 R_2} C} \qquad (27)$$
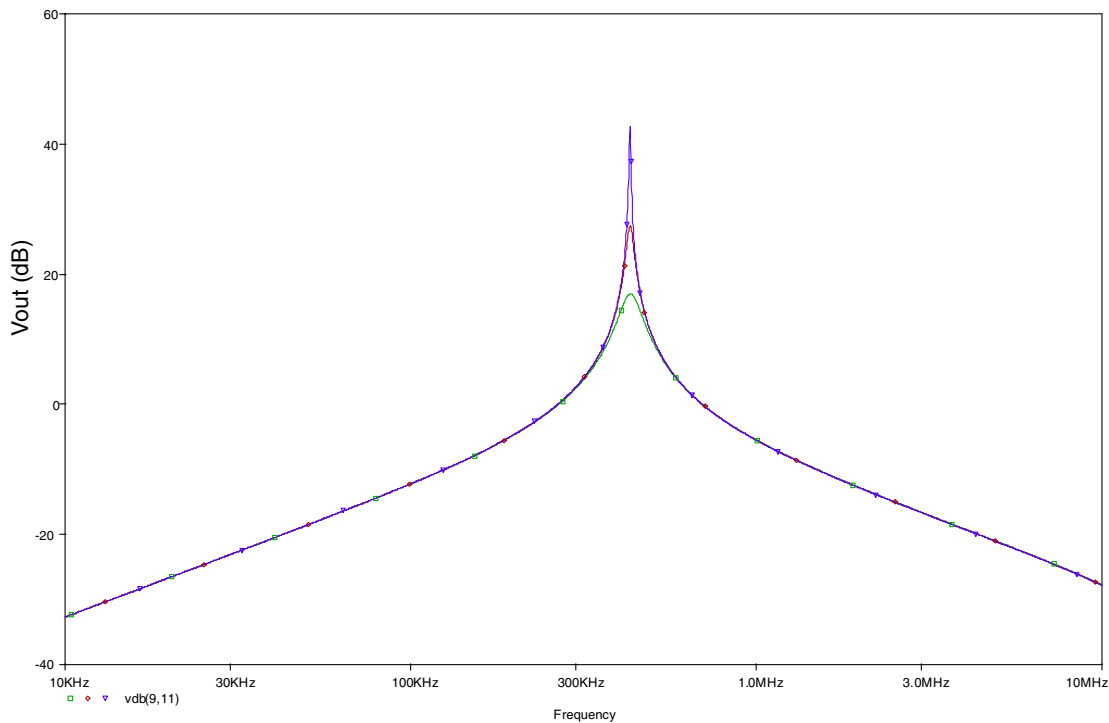
Fig. 9 Magnitude response of the second order fully differential BPF based on the proposed FDCCII

$$Q = \frac{1}{2}\sqrt{\frac{R_2}{R_1}} \tag{28}$$

$$|H| = \frac{1}{2}\frac{R_3}{R_1} \tag{29}$$

Therefore, it is possible to achieve high Q by proper selection of R_2 and R_1. The center frequency can be tuned without disturbing Q by simultaneously programming C_1 and C_2 using capacitor arrays [13]. One more advantage of this filter is that its gain H can be programmed without disturbing the center frequency and the quality factor by changing R_3.

Figure 9 shows the simulated frequency response of the bandpass filter shown in Fig. 8. The center frequency is 455 KHz, Quality factor is tuned from 5 to 20 and its gain is tuned from 17 to 42 dB.

4 Conclusion

A CMOS FDCCII has been introduced, analyzed and simulated. The FDCCII is based on a fully differential difference transconductor circuit as an input stage and two class AB output stages. The circuit is suitable for wide range, low voltage and low power applications. For proper operation of the proposed FDCII common mode feedback circuits is used to control the common mode value of the X-terminals and the Z-terminals [14]. The proposed FDCCII circuit is characterized by the ability to achieve high gain with low loss of bandwidth. Application examples in designing variable gain amplifier (VGA), fully differential integrator, and second order bandpass filter are also provided. The realization of the proposed FDCCII is different from the realization proposed in [15] in which the FDCII is based on the current sensing of differential difference amplifier. Also the realization given in [16] is based on fully differential buffer in the input stage. Finally the realization given in [17] is different from the proposed FDCII because it has three Y terminal and only one X terminal.

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