NEW CMOS BALANCED OUTPUT TRANSCONDUCTOR AND APPLICATION TO GM-C BIQUAD FILTER

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ABSTRACT

A new CMOS voltage controlled balanced output transconductor (BOTA) is introduced. Application of the CMOS BOTA in realizing mixed-mode filter implementation featuring electronic tunability is presented. The filter realizes second order lowpass, bandpass, highpass, allpass and notch responses. The proposed filter architecture uses grounded capacitors and allows modifying the quality factor without changing the center frequency. PSpice simulations are given to confirm the theoretical analysis.

1. INTRODUCTION

The programmable balanced output transconductor is a useful building block for continuous-time analog signal processing. Several realizations for the CMOS transconductors with single or multiple outputs and their applications have been introduced in the literature [1-4]. These realizations can be categorized into four main classes; the first class is based on using a differential stage with MOS transistors operating in the saturation region [1]. The second class is based on the use of MOS transistors operating in the non-saturation region [2]. The third class comprises transconductors that use both differential stage and MOS transistors operating in the non-saturation region [3]. The fourth class is based on using MOS transistors operating in the saturation region with the help of biasing circuits to obtain the linear relation between the output current and the input voltage [4].

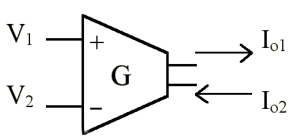

Figure 1 Symbol of the BOTA.

In this paper a new CMOS realization of a BOTA based on transistors operating in the saturation region is given. The proposed BOTA is insensitive to threshold voltage variation. The proposed BOTA can be programmed using a control voltage, which allows the compensation of the process parameter spreads in automatically tuned filters. The BOTA, whose symbol is shown in Fig. 1, has two input voltages and provides two balanced currents through the two output terminals.

The application of the BOTA in realizing mixed-mode biquad filter is given. The filter implementation is capable of realising lowpass, bandpass, highpass, allpass and notch responses using three BOTAs and two grounded capacitors, which makes the filter suitable for VLSI. The quality factor of the proposed filter can be tuned independently of the center frequency. In section 2, the realization of the programmable CMOS balanced output transconductor is presented. In section 3, the application of the BOTA in realising mixed-mode filter is given. PSpice simulations are included to illustrate the linearity range of the transconductor circuit, the high performance of the proposed filter as well as to verify the analytical results.

2. THE PROPOSED BALANCED OUTPUT TRANSCONDUCTOR CIRCUIT

The proposed CMOS balanced output transconductor circuit is shown in Fig. 2. The matched transistors M1 through M4 are the basic transistors and their gate voltages are the input voltages to the transconductor. The circuit formed of transistor M9 through M24 is used to generate a biasing voltage V_S, which is a linear function of the control voltage V_C and the summation of the two input voltages. The voltage V_S is used to bias the common source of the four basic transistors allowing to obtain a linear function between the output currents and the input voltage when the currents flowing through the four basic transistors are subtracted by means of the two current mirrors (M5-M6 and M7-M8). The transconductor output currents are obtained as follows:

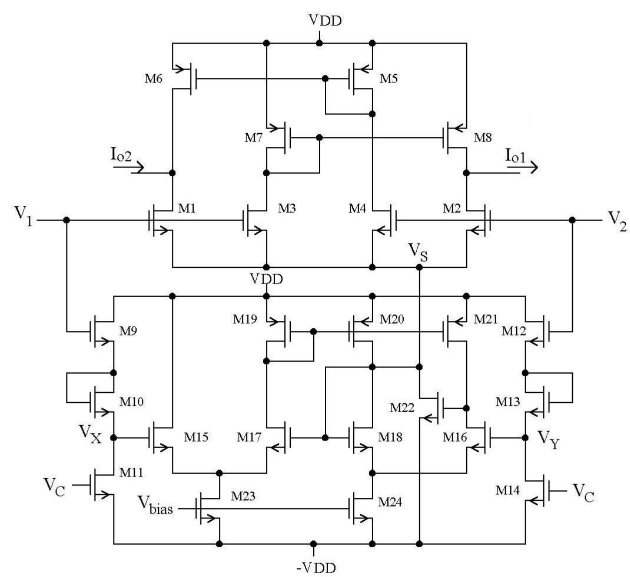

Figure 2 The CMOS realization of the BOTA.

Assuming all transistors are operating in the saturation region, the currents flowing through the matched transistors M1 through M4 can be written as follows:

$$I_1 = I_3 = \frac{K_1}{2}(V_1 - V_S - V_{Tn})^2 \tag{1}$$

$$I_2 = I_4 = \frac{K_1}{2}(V_2 - V_S - V_{Tn})^2 \tag{2}$$

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Where $K_i = \mu_n C_{ox} (\frac{W}{L})_i$, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W/L is the aspect ratio and V_{Tn} is the threshold voltage of the i^{th} transistor.

The transistors M9 to M11 and M12 to M14 are level shifter circuits used to shift the two input voltages V_1 and V_2 to the new voltages V_X and V_Y respectively. The control voltage V_C is included to control the level shifts in the input signals. Assuming that $K_9 = K_{10} = 4 K_{11}$ and $K_{12} = K_{13} = 4 K_{14}$, the voltages V_X and V_Y are given by:

$$V_X = V_1 - V_C - V_{DD} - V_{Tn} \tag{3}$$

$$V_Y = V_2 - V_C - V_{DD} - V_{Tn} \tag{4}$$

The circuit formed from M15 to M24 is used to generate the biasing voltage V_S. The current sources transistors M23 and M24 force equal tail currents into the two differential pairs formed by M15-M17 and M16-M18. The current flowing through M17 is mirrored to M16 by the action of the current mirror M19-M21. Since the summation of I_{15} and I_{17} is equal to that of I_{16} and I_{18}, hence, M15 and M18 will have equal currents. Assuming that M15 through M18 are matched transistors, V_{GS15} will be equal to V_{GS18} and also V_{GS16} will be equal to V_{GS17}, resulting in the following relations:

$$V_X - V_{S15} = V_S - V_{S18} \tag{5}$$

$$V_X - V_{S18} = V_S - V_{S15} \tag{6}$$

From (3) to (6), the biasing voltage V_S can be written as:

$$V_S = \frac{1}{2} (V_1 + V_2 - 2V_C - 2V_{DD} - 2V_{Tn}) \tag{7}$$

The two current mirrors M5-M6 and M7-M8 are used to obtain the two output currents from the basic four transistors. Referring to the currents directions given in Fig. 2 and from (1) and (2), the output currents are given by:

$$I_{o1} = I_{o2} = I_1 - I_2 \tag{8}$$

From (1) to (8), the transconductor output currents are obtained as follows:

$$I_{o1} = I_{o2} = K_1 (V_C + V_{DD}) (V_1 - V_2) \tag{9}$$

As given by (9), the proposed CMOS circuit shown in Fig. 2 operates as a linear balanced output transconductor with a programmable transconductance G that is controlled by the control voltage V_C and is given by:

$$G = K_1 (V_C + V_{DD}) \tag{10}$$

PSpice simulations were carried out to verify the performance of the proposed BOTA circuit using model parameters of 0.5 μm CMOS process provided by MOSIS. The supply voltages were equal to ± 2.5V. Fig. 3(a) illustrates the DC transfer characteristics between the output currents of the BOTA and the input voltage V_1 for different values of V_2, where V_1 and V_2 were scanned from -1 to 1 V with V_C = -1.6 V. The variations of the output currents versus V_1 when V_2 is grounded and the control parameter V_C scanned from -1.2 to -1.6V are shown in Fig. 3(b). It is shown that the BOTA features a linear transconductance gain over the input range from -1 to 1 V and that the control voltage V_C can be used to vary the transconductance gain from 119 μA/V to 171 μA/V. Figs. 3(c) and 3(d) indicate that both the magnitude and phase responses of the BOTA output current are flat up to 10MHz. The bandwidth of the output current was equal to 78 MHz. The BOTA output resistance (R_{out}) and output capacitance (C_{out}) were found to be 2.6 MΩ and 0.045 pF respectively. The power consumption of the overall transconductor was less than 4 mW for biasing currents of 300 μA flowing through M23 and M24. PSpice simulations resulted in total harmonic distortion (THD) less than 0.25% for 1 MHz 1V peak-to-peak sinusoidal input.

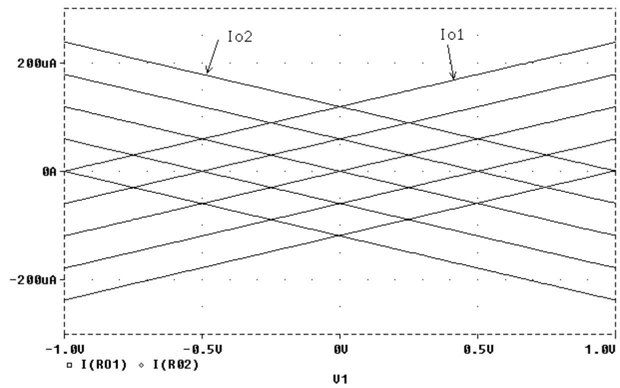

Figure 3(a) The *I-V* characteristics of the output currents of the BOTA with constant V_C. (6)

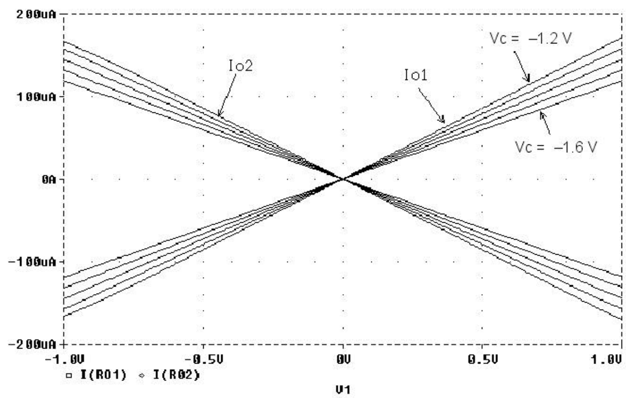

Figure 3(b) The *I-V* characteristics of of the BOTA with V_C used as a control parameter.

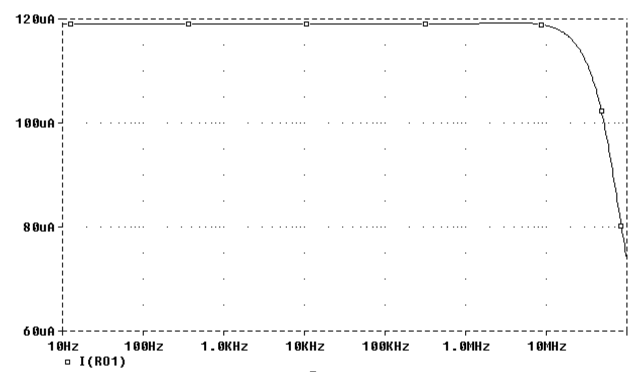

Figure 3(c) The magnitude response of the BOTA.

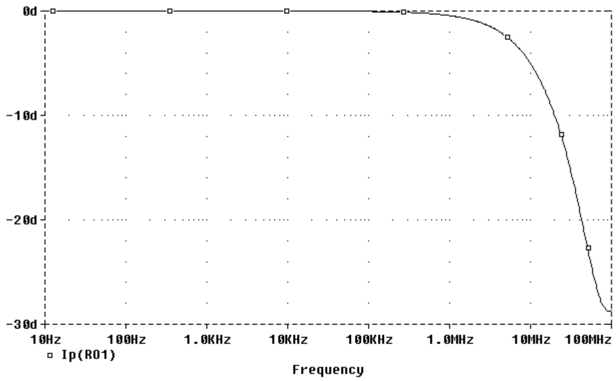

Figure 3(d) The phase response of the BOTA.

3. THE PROPOSED MIXED-MODE BIQUADRATIC FILTER

3.1 Circuit Implementation

Fig. 4(a) represents a second order filter circuit with a single input voltage, two output voltages nodes and three high impedance current output nodes. The filter simultaneously provides voltage-mode bandpass and lowpass responses as well as current-mode bandpass and highpass responses. The allpass and notch responses can also be obtained by adding two of the three output currents. The circuit uses only three BOTAs and two grounded capacitors, which makes the filter suitable for VLSI implementation. By direct analysis, the following voltage-mode transfer functions are obtained:

$$\frac{V_{BP}}{V_i} = \frac{\frac{-G_1}{C_1}s}{D(s)} \tag{11}$$

$$\frac{V_{LP}}{V_i} = \frac{\frac{G_1G_3}{C_1C_2}}{D(s)} \tag{12}$$

Where

$$D(s) = s^2 + \frac{G_2 - G_1}{C_1}s + \frac{G_2G_3}{C_1C_2} \tag{13}$$

Referring to the current directions shown in Fig. 4(a), the following output currents are also obtained:

$$\frac{I_{o1}}{V_i} = \frac{G_1\left(s^2 + \frac{G_2}{C_1}s + \frac{G_2G_3}{C_1C_2}\right)}{D(s)} \tag{14}$$

$$\frac{I_{o2}}{V_i} = \frac{G_2\left(\frac{G_1}{C_1}s + \frac{G_1G_3}{C_1C_2}\right)}{D(s)} \tag{15}$$

$$\frac{I_{o3}}{V_i} = \frac{\frac{G_3G_1}{C_1}s}{D(s)} \tag{16}$$

The highpass response is obtained by adding the output currents of the two transconductances G_1 and G_2 in Fig. 4(a), hence, the following transfer function is obtained:

$$\frac{I_{o4}}{V_i} = \frac{I_{o1} - I_{o2}}{V_i} = \frac{G_1 s^2}{D(s)} \tag{17}$$

Similarly, adding the output currents of the two transconductances G_1 and G_3 in Fig. 4(a) results in the general biquadratic transfer function:

$$\frac{I_{o5}}{V_i} = \frac{I_{o1} - I_{o3}}{V_i} = \frac{G_1\left(s^2 + \frac{G_2 - G_3}{C_1}s + \frac{G_2G_3}{C_1C_2}\right)}{D(s)} \tag{18}$$

From (18), the notch response can be obtained by setting $G_2 = G_3$, while the allpass response is obtained by making $G_3 = 2G_2 - G_1$. These conditions can be easily satisfied by adjusting the control voltage V_C of the transconductors used.

From the above equations, the design equations of the filter are given by:

$$w_o = \sqrt{\frac{G_2G_3}{C_1C_2}} \tag{19}$$

$$Q = \frac{G_2}{G_2 - G_1}\sqrt{\frac{C_1G_3}{C_2G_2}} \tag{20}$$

It is seen that the transconductance G_1 controls the quality factor of the filter (Q) without affecting the center frequency (ω_o). Moreover, high Q values can be obtained by adjusting the difference between G_2 and G_1, hence, avoiding large spread in the transconductance values.

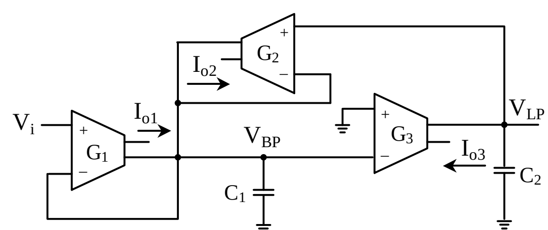

Figure 4(a) The first proposed BOTA-C active filter.

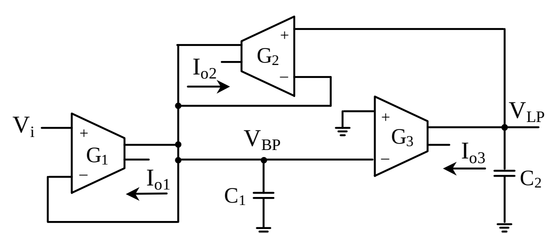

Figure 4(b) The modified version of the BOTA-C filter.

From (20) and considering the case when Q values less than unity are desirable; such as the case of designing a maximally flat lowpass response, in this case, if equal C design is chosen, the value of G_3 must be chosen smaller than G_2. However, this constraint disallows the realization of the notch and allpass responses as described by (18). It is worth noting that this constraint is present only when equal C design is desirable and it can be avoided by reversing the polarity of G_1 in the design equations. This can be done by interchanging the two output currents of G_1 as shown in Fig. 4(b). The corresponding transfer functions and design equations of the modified filter are similar to those given by (11) to (20) but after inverting the sign of G_1. Hence, the modified filter of Fig.4(b) offers all the responses obtained from the filter of Fig. 4(a) with notch and allpass responses featuring Q values less than unity.

3.2 Simulation Results

The design of the filter of Fig. 4(a) to realize a second-order bandpass response with quality factor equal to 21, and center frequency of 1 MHz is given. The value of the two equal capacitors C_1 and C_2 is equal to 7.2 pF. The transconductances values were taken as follows: $G_2 = G_3 = 42$ μA/V and $G_1 = 40$ μA/V. Fig. 5(a) shows the magnitude response of the bandpass filter with errors in ω_o and Q less than 1%. PSpice simulations were also performed using the filter of Fig. 4(b) to realize a maximally flat lowpass response designed at a center frequency of 1 MHz with $C_1 = C_2 = 7.2$ pF, $G_1 = 18.5$ μA/V and $G_2 = G_3 = 42$ μA/V. The magnitude response of the lowpass filter is shown in Fig. 5(b) and the error in ω_o was less than 1%. Figs. 5(c) and 5(d) represent the current-mode notch response obtained using the filter of Fig. 4(a). The filter was designed to realize Q of 21 and center frequency of 1 MHz by taking $C_1 = C_2 = 7.2$ pF, $G_1 = 36$ μA/V, $G_2 = 40$ μA/V and $G_3 = 44$ μA/V. As shown in Figs. 5(c) and 5(d), small shifts in ω_o and Q (less than 1%) were obtained.

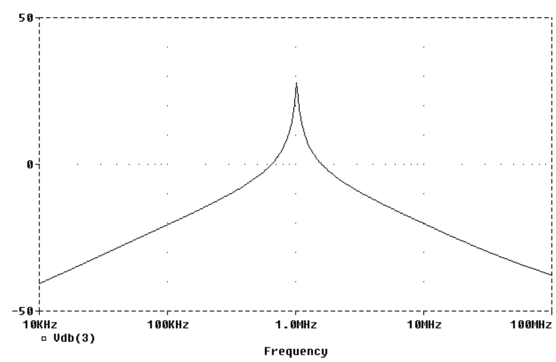

Figure 5(a) The magnitude response of the voltage-mode bandpass output

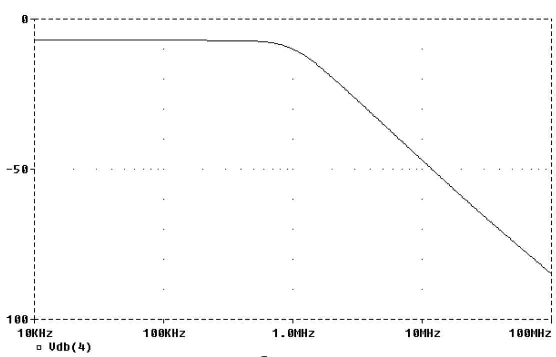

Figure 5(b) The magnitude response of the voltage-mode lowpass output.

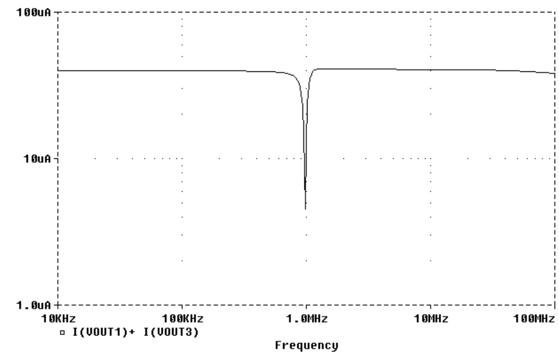

Figure 5(c) The magnitude response of the current-mode notch output.

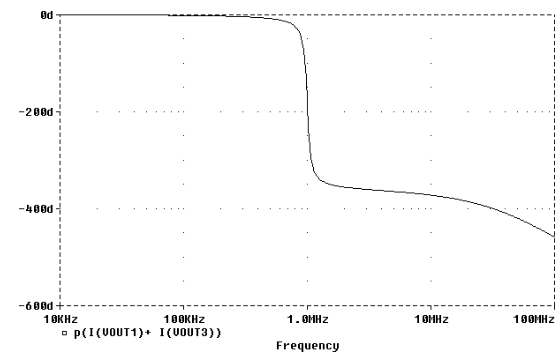

Figure 5(d) The phase response of the current-mode allpass output.

4. SUMMARY

A new CMOS linear balanced output transconductor has been proposed. Application of the BOTA in realizing second-order mixed-mode active filter was given. The filter has single input voltage and three output currents and is capable of providing lowpass, bandpass, highpass, allpass and notch responses using three transconductances and two grounded capacitors. The attractive feature of the proposed filter is that the control of Q is independent of the center frequency ω_o. PSpice simulations of the proposed BOTA and for its application were also included. It was shown that the simulation results are in good agreement with the analytical analysis.

5. REFERENCES

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