Analog Integrated Circuits and Signal Processing, 43, 61–69, 2005

Fully Differential CMOS Current Feedback Operational Amplifier

SOLIMAN A. MAHMOUD AND INAS A. AWAD

Electronics and Communications Engineering Department, Cairo University, Fayoum Branch, Egypt

Received October 6, 2003; Revised February 27, 2004; Accepted April 21, 2004

Abstract. This paper presents a new CMOS fully differential current feedback operational amplifier (FDCFOA). The proposed CMOS realization of the FDCFOA is based on a novel class AB fully differential buffer circuit. Besides the proposed FDCFOA circuit is operating at supply voltages of ± 1.5 V, it has a total standby current of 400 μA. The applications of the FDCFOA to realize variable gain amplifier, fully differential integrator, and fourth order fully differential maximally flat low pass filter are given. The fourth order filter provides 8 dB gain and a bandwidth of 4.3 MHz to accommodate the wideband CDMA standard. The proposed FDCFOA and its applications are simulated using CMOS 0.35 μm technology.

Key Words: current feedback opamp, fully differential buffer, current conveyor

1. Introduction

In recent years, fully differential circuit configurations have been widely used in high-frequency analog signal applications like switched capacitor filters [1] and multi-standard wireless receivers [2]. As compared to their single-ended counterparts, they have higher rejection capabilities to clock-feed-through, charge injection errors and power–supply noises, larger output dynamic range, higher design flexibility, and reduced harmonic distortion. In this paper, a new fully differential CMOS current feedback amplifier (FDCFOA) is proposed. The proposed CMOS realization of the FDCFOA is based on a novel class AB fully differential buffer circuit. The FDCFOA has the advantages of the single ended CFOA beside the advantages of the fully differential signal processing. The FDCFOA has many useful applications like the single ended CFOA [3–13].

The FDCFOA is basically a fully differential device as shown in Fig. 1. The Y_1 and Y_2 terminals are high impedance terminals while the X_1 and X_2 terminals are low impedance ones. The differential input voltage V_{Y12} applied across Y_1 and Y_2 terminals is conveyed to a differential voltage V_{X12} across the X_1 and X_2 terminals; i.e., ($V_{X12} = V_{Y12}$). The input currents applied to the X_1 and X_2 terminals are conveyed to the Z_1 and Z_2 terminals, i.e., ($I_{x1} = I_{z1}$ and $I_{x2} = I_{z2}$). The Z_1 and Z_2 terminals are high impedance output nodes suitable for current outputs. The differential voltage developed across the Z_1 and Z_2 terminals is buffered by a unity gain fully differential voltage buffer to the output terminals O_1 and O_2, i.e., ($V_{O12} = V_{Z12}$). The block diagram of the FDCFOA is shown in Fig. 2. The input stage FDB1 is a unity gain fully differential buffer forcing V_{X12} to follow V_{Y12}. The input currents to the X_1 and X_2 terminals are transferred to the high impedance nodes Z_1 and Z_2 terminals by means of current mirrors. The differential output voltage is obtained by using a second fully differential unity gain buffer FDB2. Therefore, the structure of the FDCFOA is based on using two FDBs and current mirrors.

The paper is organized as follows, in Section 2, the realization of the FDCFOA is presented. In Section 3, applications of the FDCFOA in realizing fully differential integrator, fourth order fully differential maximally flat low pass filter consisting of two cascaded biquad sections are given. PSpice simulations of the proposed FDCFOA and its applications using CMOS 0.35 μm technology are also given.

2. CMOS Realization of the FDCFOA

The structure of the proposed FDCFOA is based on the proposed class AB fully differential buffer (FDB) circuit shown in Fig. 3. The proposed FDB is consisting

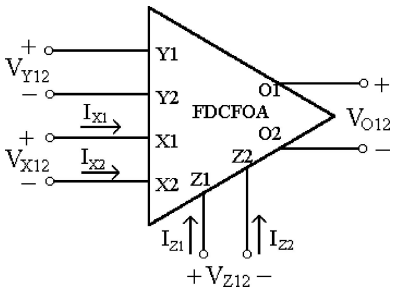

Fig. 1. The symbol of the FDCFOA.

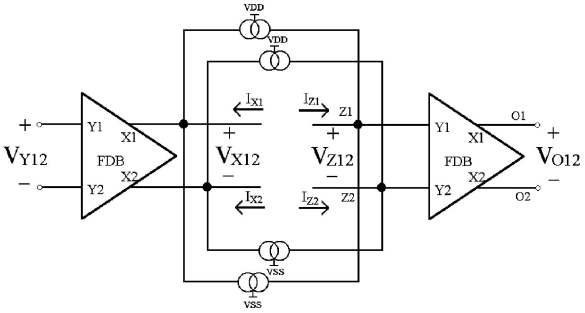

Fig. 2. The block diagram of the FDCFOA.

of two matched differential pairs (M1, M2) and (M3, M4), two pairs of matched biasing current source transistors (M5, M6) and (M7, M8), two class AB output stages (M9 to M12) and (M13 to M16) and the biasing of the output stages (M17 to M19). The differential input is applied to the two high impedance terminals of the NMOS transistors M3 and M2.

M7 and M8 carry equal bias currents (I_B) while the equal bias currents flowing through M5 and M6 are set to ($I_B/2$). Therefore:

$$I_{M1} + I_{M2} = I_{M3} + I_{M4} \tag{1}$$

$$I_{M2} = I_{M3} \tag{2}$$

From the above equations it follows that $I_{M1} = I_{M4}$. Hence, the matched differential pair transistors carry equal differential and common mode current values. Therefore,

$$V_{o+} - V_{o-} = V_{i+} - V_{i-} \tag{3}$$

To maintain a good current drive capability with low output impedance outputs, class AB output stages are used. Transistors (M11, M12) and (M15, M16) form the push pull output stage transistors. The level shift circuits formed by (M9, M10) and (M13, M14) are used to realize controlled floating voltage sources that controls the standby current through the output stage transistors. The standby current is adjusted by the biasing circuit formed of M17, M18, and M19. The standby power consumption of the overall circuit for dual power supply is given by:

$$P_{SB} = 2\,V_{DD}(3\,I_{SB} + 2\,I_B + K_9\,(V_{DD} - V_{Tn} + V_{Tp})^2) \tag{4}$$

The last term in the above equation is the current through the level shift transistors (M9, M10) and (M13,

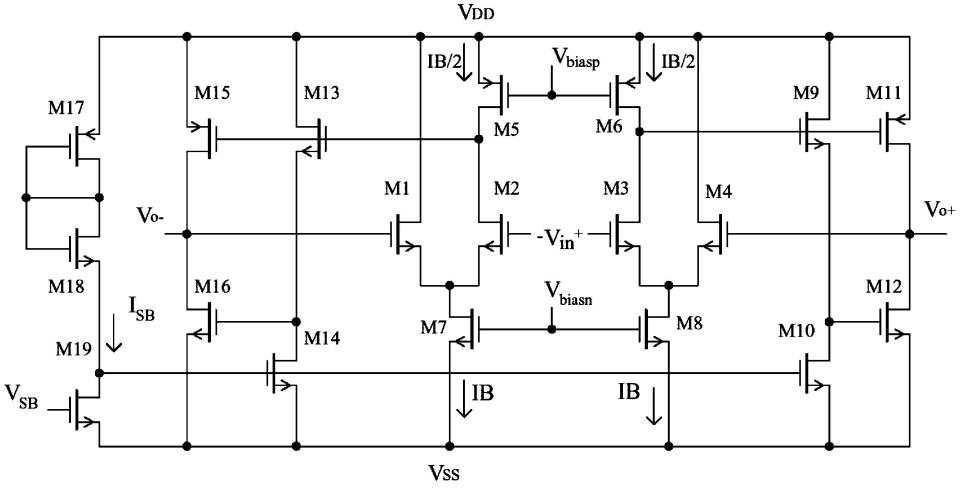

Fig. 3. The CMOS circuit of the FDB.

M14). This current can be kept small by choosing a small aspect ratio for (M9, M10) and (M13, M14). The class AB output stage enables the circuit to derive heavy resistive and capacitive load with low standby power dissipation and no slewing. It is worth mentioning that smaller miller compensation capacitors can be connected between the gate and drain of transistors M11 and M15 to ensure good transient response under all load conditions.

To prevent the drift in the output common mode (CM) voltage, a common mode feedback (CMFB) circuit is needed. It determines the output CM voltage and controls it to a specified value V_{cm} (usually mid-rail) even with the presence of large differential signals. When dual power supplies are used V_{cm} is set to zero Volt. The CMFB circuit consists of transistors Mcm1 to Mcm10 as shown in Fig. 4 in addition to two resistors (R_{cm}) and two capacitors (C_{cm}) which are used to control the CM voltage of the outputs (V_{o+} and V_{o-}). Transistors Mcm1 and Mcm2 are employed to isolate the CMFB circuit from the basic circuit. This is essential to make the input current of the CMFB circuit equal to zero. The CMFB circuit generates the CM voltage of the output signals at node V_{oav} via the two equal resistors (R_{cm}). This voltage is then compared to V_{cm} using differential amplifier Mcm3 and Mcm4 with negative feedback forcing V_{oav} to follow V_{cm}.

The operation of the CMFB circuit can be explained as follows. Assuming the ideal case of fully balanced output signals; i.e., $V_{oav} = 0$. Since V_{oav} and V_{cm} are equal, the tail current ($I_B/2$) will be divided equally between Mcm3 and Mcm4. Therefore, a current $I_B/4$ will be passed via Mcm5, Mcm6 and Mcm7 to the output nodes and the circuit exhibits the proper biasing even

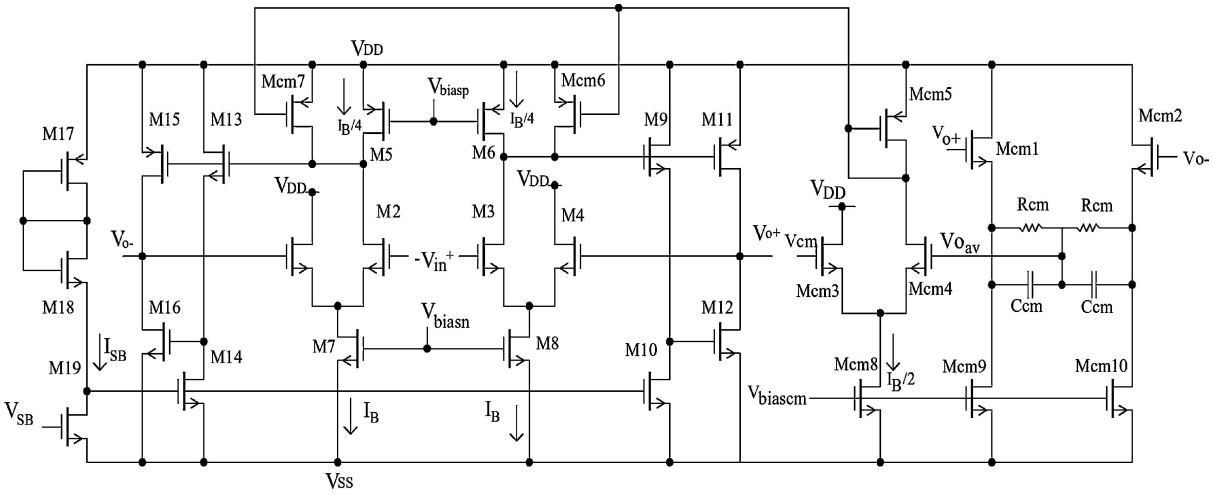

Fig. 4. The CMOS circuit of the FDB with CMFB circuit.

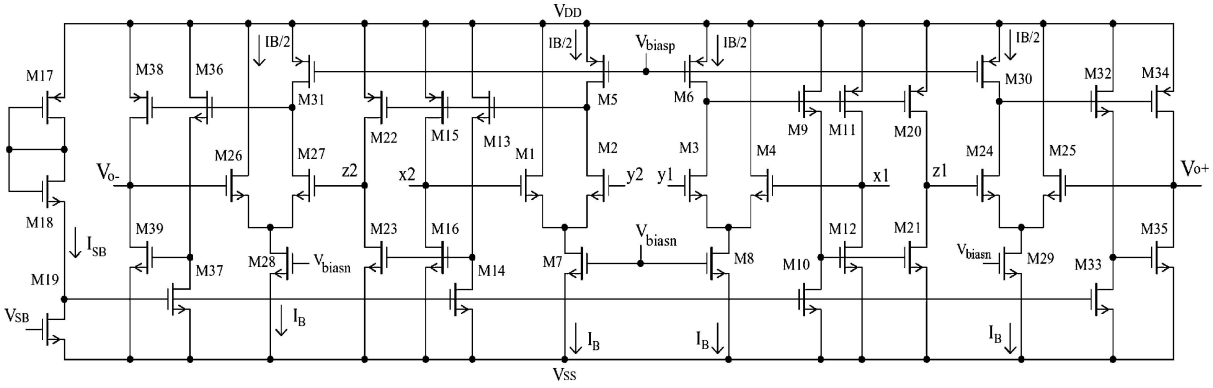

Fig. 5. The CMOS circuit of the FDCFOA.

when large differential signals are present. Next consider the case when the magnitude of V_{o+} is greater than V_{o-} which results in a positive CM signal at V_{oav}. This voltage will cause the current in Mcm6 and Mcm7 to increase pulling down the voltages V_{o+} and V_{o-} until the CM voltage V_{oav} is brought back to zero. Similarly, in the case of a negative CM signal, the loop will adjust the V_{oav} to be equal to V_{cm}.

From the block diagram of FDCFOA in Fig. 2, the overall CMOS circuit of the FDCFOA without the common mode feedback circuit is shown in Fig. 5.

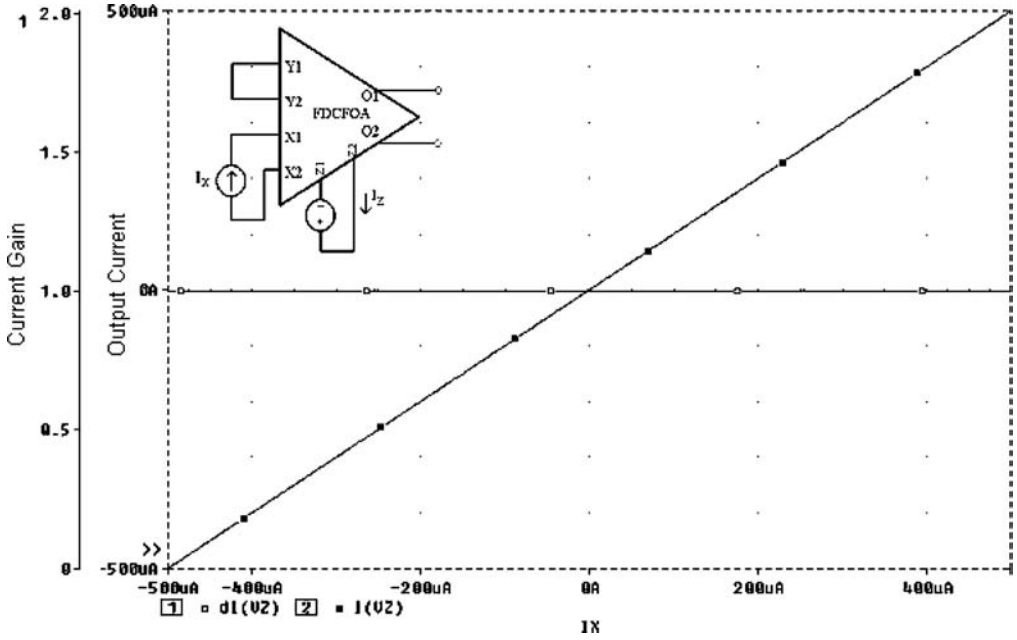

Fig. 6. The variations of the output current I_Z and its transfer gain with respect to the input current I_X.

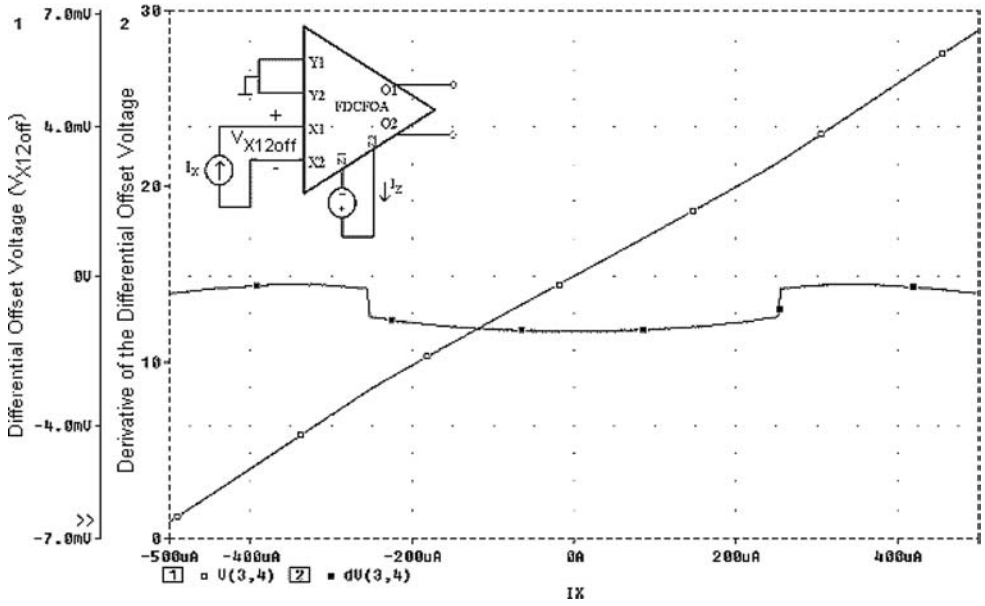

Fig. 7. The differential offset voltage across the X_1 and X_2 terminals along with its derivative.

The performance of the proposed FDCFOA circuit was verified by performing PSpice simulations with supply voltages ± 1.5 V and using 0.35 μm CMOS technology parameters. Figure 6 shows the floating output current across the Z_1 and Z_2 terminals when a floating input current I_X is connected across the X_1 and X_2 terminals and scanned from -500 to 500 μA while the differential voltage across Y_1 and Y_2 is set to zero. It has been found that the magnitude of I_Z follows that of I_X with a maximum output current of 5 mA with a

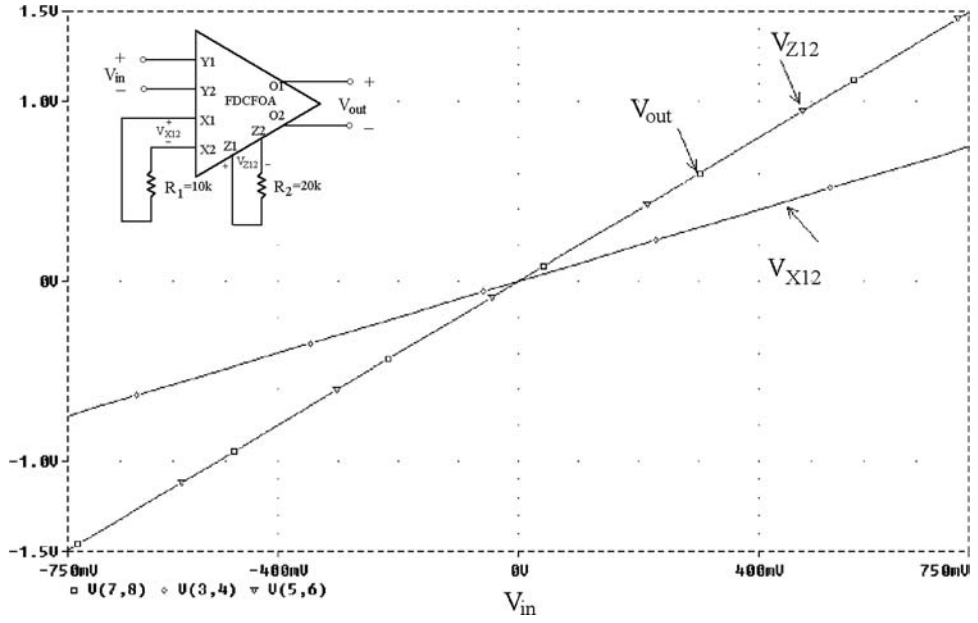

Fig. 8. The voltage swings V_{X12}, V_{Z12} and V_{out} of the FDCFOA based amplifier.

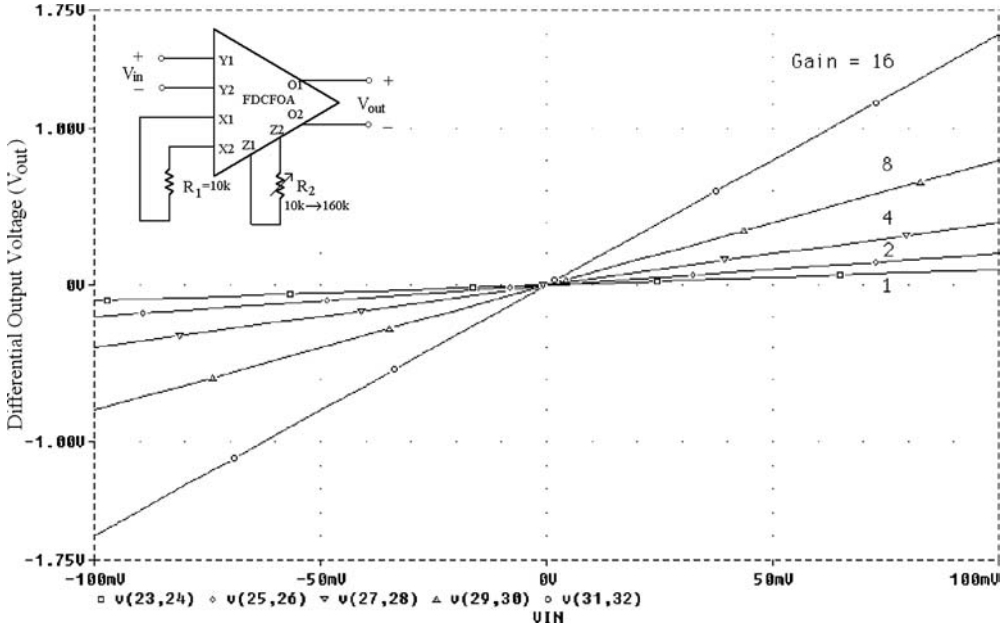

Fig. 9. The DC transfer characteristics of the FDCFOA based variable gain amplifier for different values of R_2.

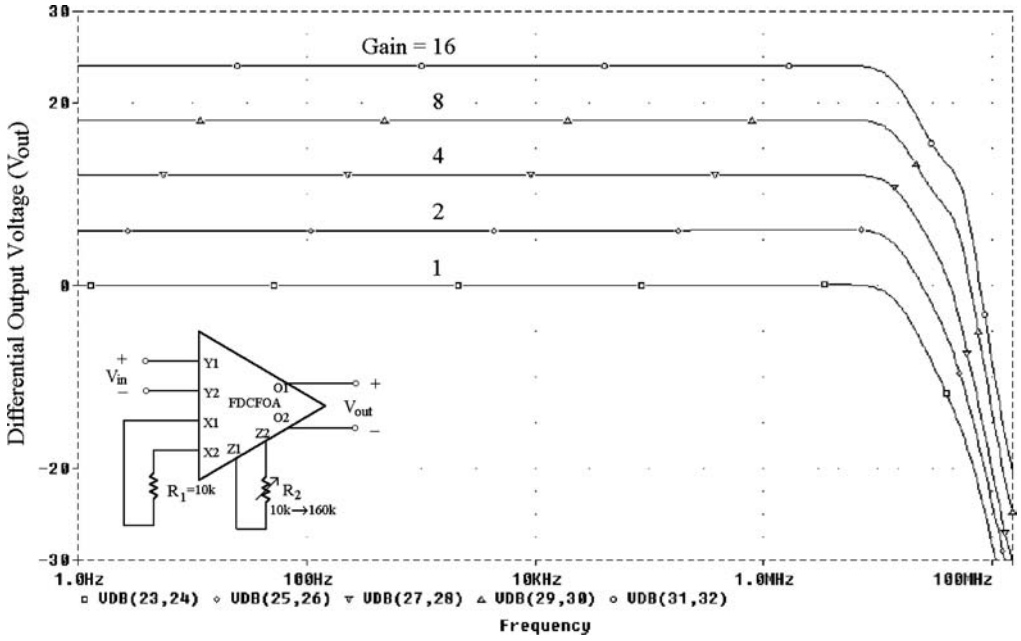

Fig. 10. The frequency response of the FDCFOA based variable gain amplifier.

gain error of 0.03% for a 2 mA output current. Figure 7 shows the variations of the offset voltage across the X1 and X2 terminals versus the variation in the input current applied across X1 and X2 (I_X) when the V_{Y12} is equal to zero. The differential X input resistance (R_{X12}) is less than 20 Ω. The offset voltage is less than 7 mV at $I_z = 500\ \mu A$. Figure 8 shows the voltage swings V_{X12}, V_{Z12} and V_{O12} when the FDCFOA is used to realize a voltage amplifier with gain of two. The maximum input common mode voltage is equal to 0.75 V and the common mode voltage of the output is forced by the CMFB circuit to zero Volt. The maximum DC differential voltage gain error is found to be less than 0.01% for a 0.75 V differential input. The maximum differential output voltage is equal to 2.4 V. The power supply rejection ratio (PSRR) from positive supply to the output is 92 dB and from negative supply is 96 dB. The differential DC characteristics of the FDCFOA based variable gain amplifier (VGA) for different gain values is shown in Fig. 9. Also, the frequency response of the FDCFOA based variable gain amplifier is shown in Fig. 10. It is clear from Fig. 10 that the VGA based on the FDCFOA experiences no loss in bandwidth (which is approximately equal to 20 MHz) when the gain is increased.

3. Applications

The proposed FDCFOA can be used to implement the fully differential or fully balanced architecture of any CFOA based circuits. Two design examples are presented in this section to demonstrate the use of the proposed FDCFOA.

3.1. Fully Differential Integrator

The fully differential integrator is a basic building block in realizing continuous time filters [3, 4, 6]. Figure 11

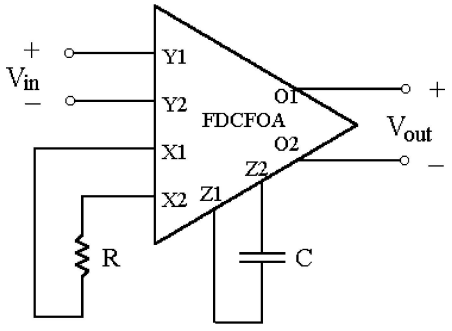

Fig. 11. The fully differential integrator.

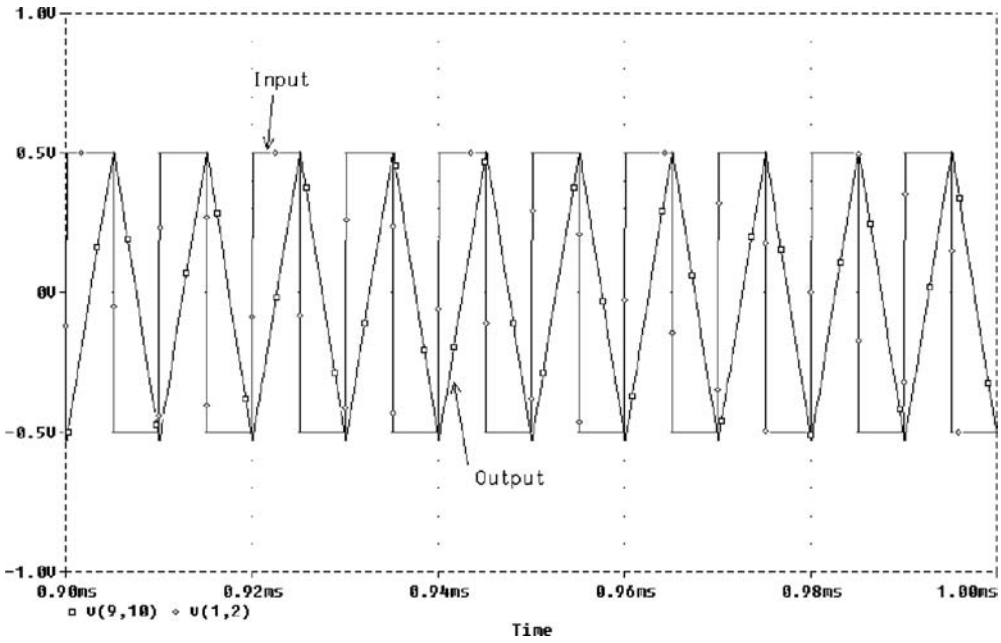

Fig. 12. The output of the integrator along with the square wave input signal.

shows the FDCFOA based fully differential integrator. The output voltage of the integrator is taken across the buffered O_1 and O_2 terminals and is given by:

$$V_O = \frac{1}{SCR} V_I \tag{5}$$

PSpice simulations results for the FDCFOA based fully differential integrator are shown in Fig. 12 with a square wave input of 1 V peak to peak amplitude and a frequency of 100 KHz, where $R = 10\,K\Omega$ and $C = 250$ pF.

3.2. FDCFOA-based Lowpass Filter

The FDCFOA is used to implement a fully differential version of the Sallen–Key filter. The filter section shown in Fig. 13 represents a filter circuit that realizes second order fully differential lowpass filter based on a single FDCFOA. By direct analysis, the following transfer function is obtained as:

$$\frac{V_O}{V_I} = \frac{\frac{K}{R_1R_2C_1C_2}}{S^2 + S\left[\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1-K}{R_2C_2}\right] + \frac{1}{R_1R_2C_1C_2}} \tag{6}$$

From the above equation, for equal R and equal C design, the ω_o, Q and the DC gain H of the filter are given

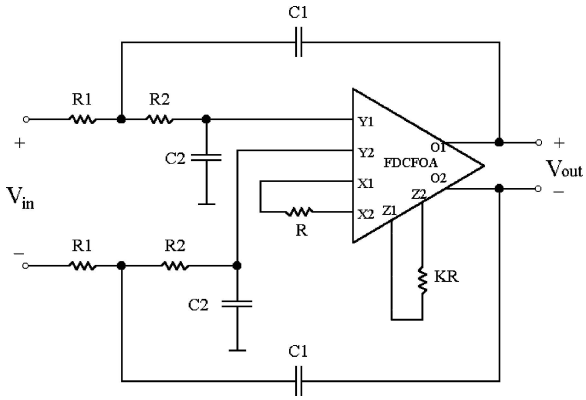

Fig. 13. The fully differential filter section based on the proposed FDCFOA.

by:

$$\omega_o = \frac{1}{RC}, \quad Q = \frac{1}{3-K}, \quad H = K \tag{7}$$

Figure 14 shows the simulated frequency response of a fourth order maximally flat lowpass filter consisting of two cascaded sections of the filter shown in Fig. 13. The fourth order filter provides 8 dB gain and a bandwidth of 4.3 MHz to accommodate the wideband

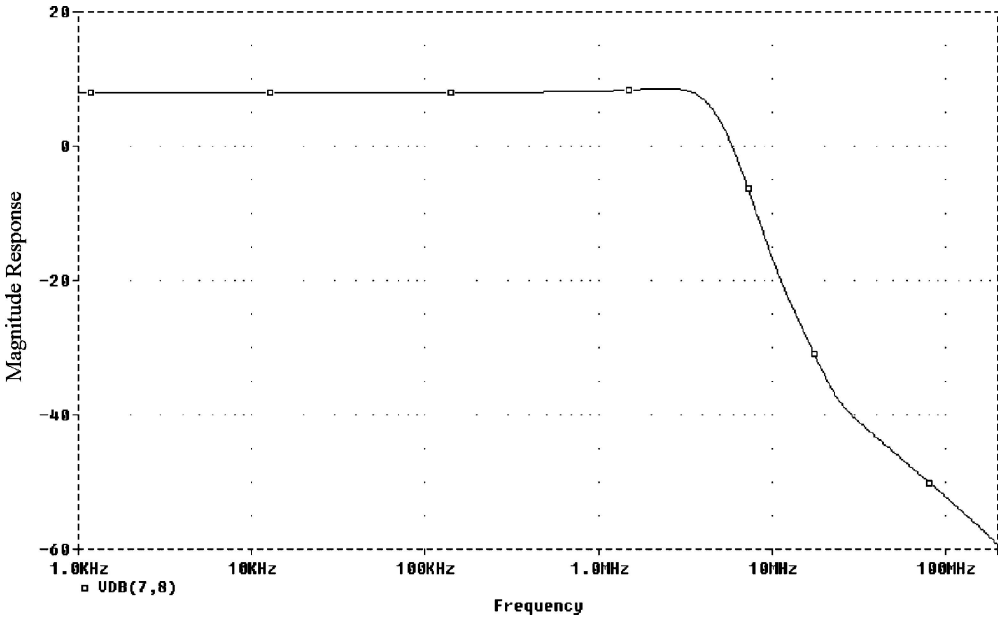

Fig. 14. The magnitude response of the fourth order fully differential filter.

CDMA standard. Also, the input referred noise of the filter circuit if found to be less than 30 nV/$\sqrt{\text{Hz}}$.

4. Conclusion

A CMOS FDCFOA has been introduced, analyzed and simulated. The FDCFOA is based on a novel class AB fully differential buffer circuit. The circuit is suitable for wide range, low voltage and low power applications. The proposed FDCFOA circuit is characterized by the ability to achieve high gain with low loss of bandwidth. Application examples in designing variable gain amplifier (VGA), fully differential integrator, and fourth order lowpass filter suitable for wideband CDMA systems are also provided.

References

1. T.C. Choi, R.T. Kaneshiro, R.W. Bodersen, P.R. Gray, W.B. Jett, and M. Wilcox, "High-frequency CMOS switched-capacitor filters communication application." *IEEE J. Solid-state Circuits*, vol. SC-18, pp. 652–663,1983.
2. H. Alzaher, H.O. Elwan, and M. Ismail, "A CMOS Fully balanced second-generation current conveyor." *IEEE Trans. On Circuits and Systems-II*, vol. 50, pp. 278–287, 2003.
3. A.M. Soliman, "Current feedback operational amplifier based oscillators." *Analog Integrated Circuits and Signal Processing*, vol. 23, pp. 45–55, 2000.
4. A.M. Soliman, "Applications of the current feedback operational amplifiers." *Analog Integrated Circuits and Signal Processing*, vol. 11, pp. 256–302, 1996.
5. S. Evans, *Current Feedback op-amp Applications Circuit Guide*. Fort Collins, CO: Complinear, 11.20–11.26, 1988.
6. S.A. Mahmoud and A.M. Soliman, "Low voltage rail to rail CMOS current feedback operational amplifier and its applications for analog VLSI." *Analog Integrated Circuits and Signal Processing*, vol. 25, pp. 47–57, 2000.
7. X.R. Meng and Z.H. Yu, "CFA based fully integrated Tow-Thomas biquad." *Electron Lett.*, vol. 32, pp. 722–723, 1996.
8. S.A. Mahmoud and A.M. Soliman, "New MOS-C biquad using the current feedback operational amplifier." *IEEE Trans. On Circuits and Systems-I*, vol. 46, pp. 1510–1512, 1999.
9. J.J. Chen, H.W. Tsao, S.I. Liu, and W. Chui, "Parastic-capacitance insensitive current mode filter using transresistance amplifier." *Proc. Inst. Elect. Eng.*, vol. 142, pp. 86–192, 1995.
10. S.A. Mahmoud and A.M. Soliman, "Novel MOS-C balanced-input balanced-output filter using the current feedback operational amplifier." *Int. J. Electron*, vol. 84, pp. 479–485, 1998.
11. E. Bruun, "A dual current feedback op amp in CMOS technology." *Analog Integrated Circuits and Signal Processing*, vol. 5, pp. 213–217, 1994.
12. S.A. Mahmoud and A.M. Soliman, "Novel MOS-C oscillators using the current feedback op-amp." *Int. J. Electron*, vol. 87, pp. 269–280, 2000.
13. S.A. Mahmoud, A.S. Elwakil, and A.M. Soliman, "CMOS current feedback op amp-based chaos generators using novel active nonlinear voltage controlled resistors with odd symmetrical characteristics." *Int. J. Electron.*, vol. 86, pp. 1441–1451, 1999.

Soliman A. Mahmoud was born in Cairo, Egypt, in 1971. He received the B.Sc. degree with honors, the M.Sc. degree and the Ph.D. degree from the Electronics and Communications Department, Cairo University—Egypt in 1994, 1996 and 1999 respectively. He is currently an Assistant Professor at the Electrical Engineering Department, Cairo University, Fayoum-Campus. His research interests include low voltage analog CMOS circuit design, filtering and applications suitable for VLSI.

Inas Awad was born in Cairo, Egypt, in 1971. She received the Bachelor, the M.Sc. and the Ph.D. degrees in Electronics and Communications from Cairo University in 1994, 1997 and 2000, respectively. In 1995, she joined the department of Electronics and Communications, Cairo University, Fayoum-Campus as a teaching assistant and now she is an Assistant Professor at the same department. Her primary research interest is in analog circuits with particular emphasis on current-mode approach and low-voltage low-power CMOS designs.