Journal of Circuits, Systems, and Computers
Vol. 14, No. 4 (2005) 667–684
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DIGITALLY CONTROLLED CMOS BALANCED OUTPUT TRANSCONDUCTOR AND APPLICATION TO VARIABLE GAIN AMPLIFIER AND GM-C FILTER ON FIELD PROGRAMMABLE ANALOG ARRAY

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Revised 2 December 2004

A digitally controlled balanced output transconductor (DCBOTA) is proposed and analyzed. The proposed DCBOTA is based on the BOTA given in Ref. 1 and MOS switches. The DCBOTA transconductance is tunable in a range of 2^{n-1} times using n bits control word. The proposed DCBOTA is simulated using CMOS 0.35 μm technology and the results have shown the feasibility of the proposed DCBOTA. The simulation results show that the DCBOTA has a transconductance tuning range from 20 μA/V to 140 μA/V using 3 bits control word and a 3-dB bandwidth larger than 80 MHz. A general configurable analog block (CAB) based on the proposed DCBOTA, capacitor array and MOS switches, is also presented. A collection of the CABs, fully differential buffers (FDBUFs), and their interconnection to construct a field programmable analog array (FPAA) is introduced. The DCBOTA is also used to realize a wide band digitally controlled variable gain amplifier (DCVGA) and six-order lowpass filter with variable gain and tunable cutoff frequency from 1 MHz to 7 MHz.

Keywords: Digital control; balanced output transconductor; VGA; GM-C filter; FPAA.

1. Introduction

Programmable characteristic of an analog cell is a key feature that is used in so many useful applications. Temperature and process variations are the main limiting problems in the field of analog VLSI. To compensate for these variations, analog and/or digital tuning of the parameters of an analog cell is employed. However, there is a limitation on the allowable range of the analog tuning voltage. Hence in these applications, digital control is attractive.[2]

In this paper, a digitally controlled balanced output transconductor (DCBOTA) is presented. The DCBOTA is based on the BOTA given in Ref. 1. The BOTA is a versatile building block for continuous time analog signal processing. Based on the BOTA circuit, CMOS floating and grounded resistors, balanced output integrators, adders, subtractors, amplifiers, GM-C active filters, and the active realization of

passive filters with minimum number of the BOTAs, and GM-C oscillators can be built.[1,3–8] The BOTA, whose symbol is shown in Fig. 1 has two voltage inputs and provide two balanced output currents through the two output terminals. The output current is given by

$$I_o = G(V_c)(V_1 - V_2)\,, \tag{1}$$

where $G(V_c)$ is the transconductance value which is controlled through the analog voltage V_c. The symbol of the proposed DCBOTA is shown in Fig. 2, where the output current is given by

$$I_o = G(V_c, d_0, d_1, \ldots, d_n)(V_1 - V_2)\,, \tag{2}$$

where $G(V_c, d_0, d_1, \ldots, d_n)$ is the transconductance value which is controlled through the analog voltage V_c and the digital word d_0, $d_1, \ldots, d_n$.

The paper is organized as follows. In Sec. 2, the realization of DCBOTA is presented. In Sec. 3, a general configurable analog block (CAB) based on the proposed DCBOTA, programmable capacitor array and MOS switches, is presented. The internal structure of a field programmable analog array (FPAA) based on the

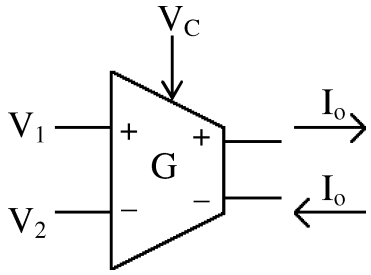

Fig. 1. The symbol of the BOTA.

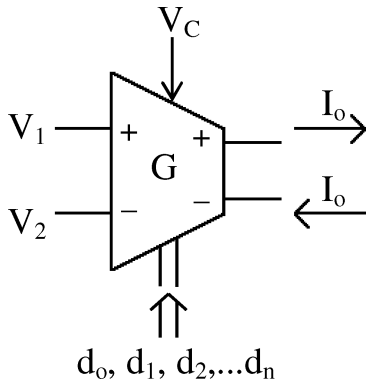

Fig. 2. The symbol of the DCBOTA.

CABs, fully differential buffers (FDBUFs) and interconnection network is also introduced. The realization of a digitally controlled variable gain amplifier (DCVGA) and six-order lowpass filter on the FPAA with variable gain and tunable cutoff frequency are given in Sec. 4.

2. CMOS Realization of the DCBOTA

The structure of the proposed DCBOTA is based on the BOTA shown in Fig. 3. The CMOS realization of the BOTA given in Ref. 1 is based on the current linearization of the basic transistors ($M1, M2, M3, M4$) by generating a suitable biasing voltages (V_a and V_b) in terms of the input voltages (V_1 and V_2) using the biasing circuit formed from transistors ($M5$ to $M16$) to bias the sources of the basic transistors and the current mirror action is performed using transistors ($M17$ to $M20$). The output current of the BOTA is given by Ref. 1 as follows:

$$I_o = 2KV_c(V_1 - V_2)\,, \tag{3}$$

where $K = \mu_n C_{ox} W/L$ is the transconductance parameter of the basic transistors, μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area and W/L is

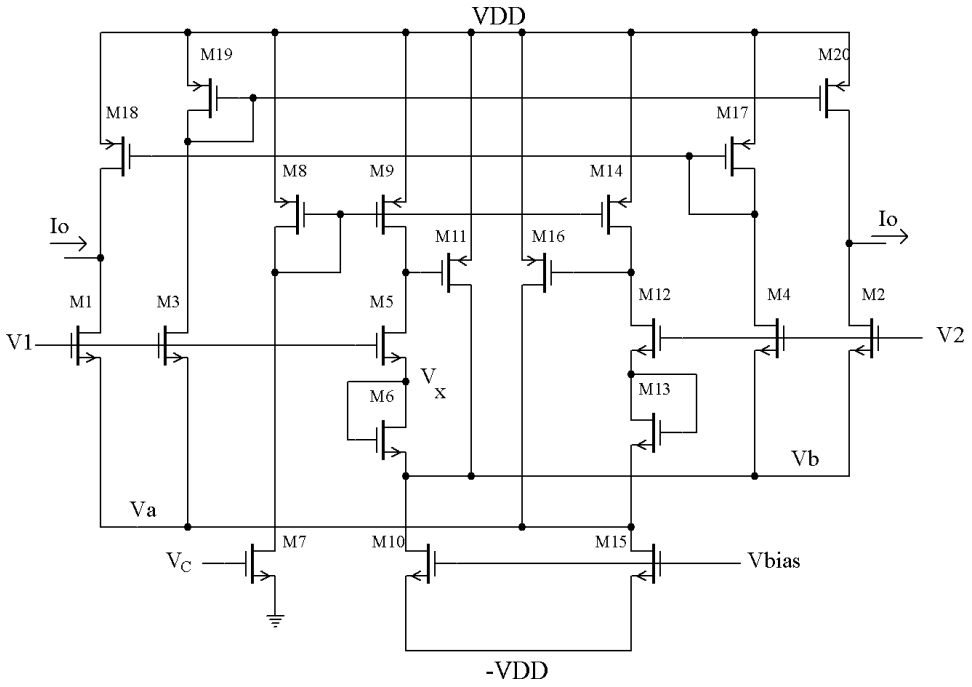

Fig. 3. The CMOS circuit of the BOTA.[1]

the aspect ratio. Therefore, the transconductance value is given by

$$G = 2KV_c\,. \tag{4}$$

Therefore, the transconductance is function of K and V_c.

The basic design idea of the proposed DCBOTA is controlling the transconductance parameter K by replacing the basic transistors with transistor arrays associated with a switches as shown in Fig. 4. The transconductance value of the proposed DCBOTA for the case of n-bit digital control word is given by

$$G = 2K(2^0 * d_0 + 2^1 * d_1 + \cdots + 2^{n*} d_n)V_c\,. \tag{5}$$

Therefore, the transconductance value can be controlled either by analog voltage V_c or digital word $(d_0, d_1, \ldots, d_n)$. As a result, the control voltage V_c affects the linearity of the transconductance,[1] the design method is based on choosing an optimum value of V_c to obtain a wide linear range and then controlling the transconductance value through the digital word. Also, for proper operation of the biasing circuits the current source formed from $M10$ and $M15$ in Fig. 3 is replaced by the digitally controlled current source shown in Fig. 4 to bias the sources of the basic transistors with a suitable biasing current depending on the control word. The standby power dissipation of the DCBOTA (P_{SBDC}) can be calculated from the following equation:

$$\begin{aligned} P_{\mathrm{SBDC}} = {} & \frac{K_7}{2}(V_c - V_t)^2 V_{\mathrm{DD}} \\ & + K_{10\,\mathrm{or}\,15}(V_{\mathrm{bias}} - V_{SS} - V_t)^2 V_{\mathrm{DD}}(2^0 * d_0 + 2^1 * d_1 + \cdots + 2^n * d_n)\,, \end{aligned} \tag{6}$$

where K_7 is the transconductance parameter of transistor M_7 and $K_{10\ \mathrm{or}\ 15}$ is the transconductance parameter of the matched transistors $M10$ and $M15$. It is worth to note that the P_{SBDC} of the DCBOTA increases for large control words compared to the P_{SB} of the BOTA, where the standby power dissipation of the BOTA is given by

$$P_{SB} = \frac{K_7}{2}(V_c - V_t)^2 V_{DD} + K_{10\ \mathrm{or}\ 15}(V_{\mathrm{bias}} - V_{SS} - V_t)^2 V_{DD}\,. \tag{7}$$

To prevent the drift in the output common mode (CM) voltage, a common mode feedback (CMFB) circuit is needed. It determines the output CM voltage and controls it to a specified value V_{cm} (usually mid-rail) even with the presence of a large differential signals. When dual power supplies are used V_{cm} is set to zero Volt. The CMFB circuit consists of transistors Mcm1 to Mcm12 as shown in Fig. 5 in addition to two resistors (R_{cm}) and two capacitors (C_{cm}) which are used to control the CM voltage of the outputs ($V_{\mathrm{o}+}$ and $V_{\mathrm{o}-}$). Transistors Mcm1 and Mcm2 are employed to isolate the CMFB circuit from the basic circuit. This is essential to make the input current of the CMFB circuit equal to zero. Therefore the output currents of the DCBOTA are not affected. The CMFB circuit generates the CM voltage of the output signals at node V_{oav} via the two equal resistors (R_{cm}). This voltage is then compared to V_{cm} using differential amplifier Mcm3 and Mcm4 with negative

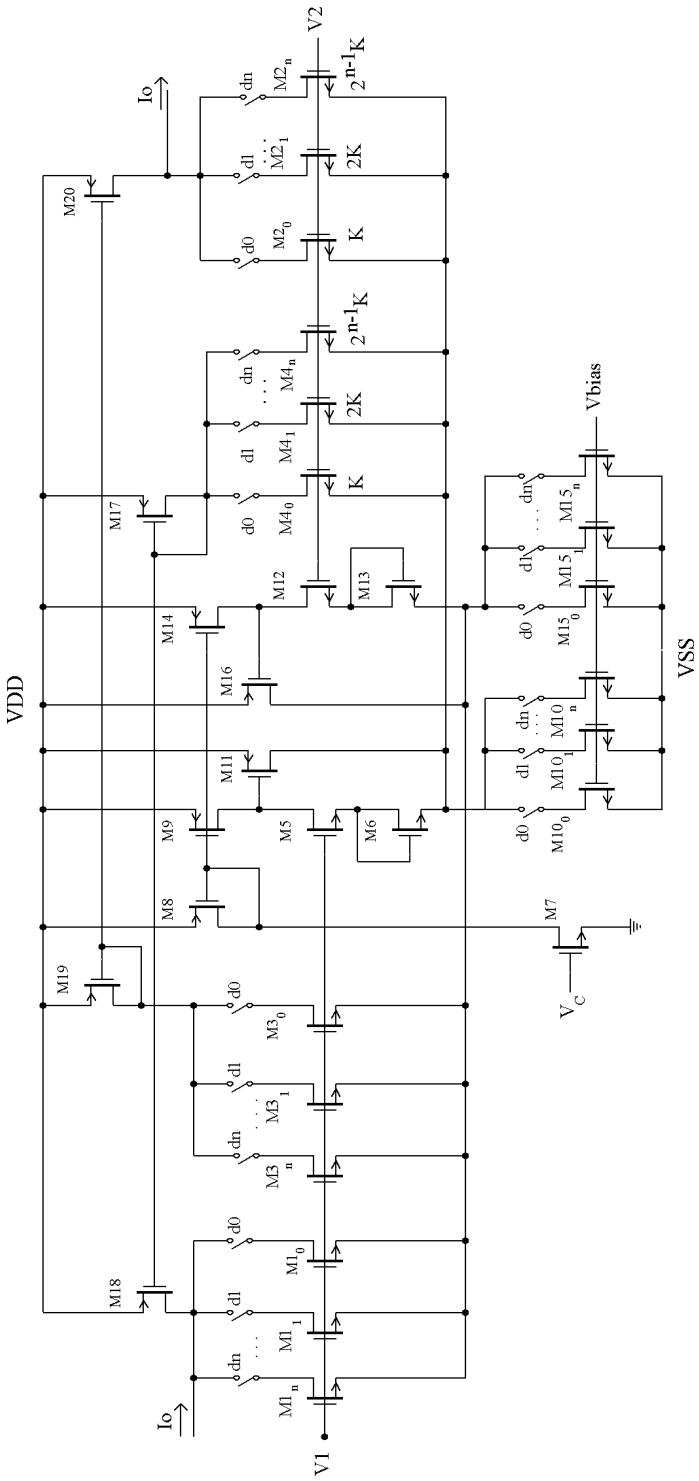

Fig. 4. The CMOS circuit of the DCBOTA.

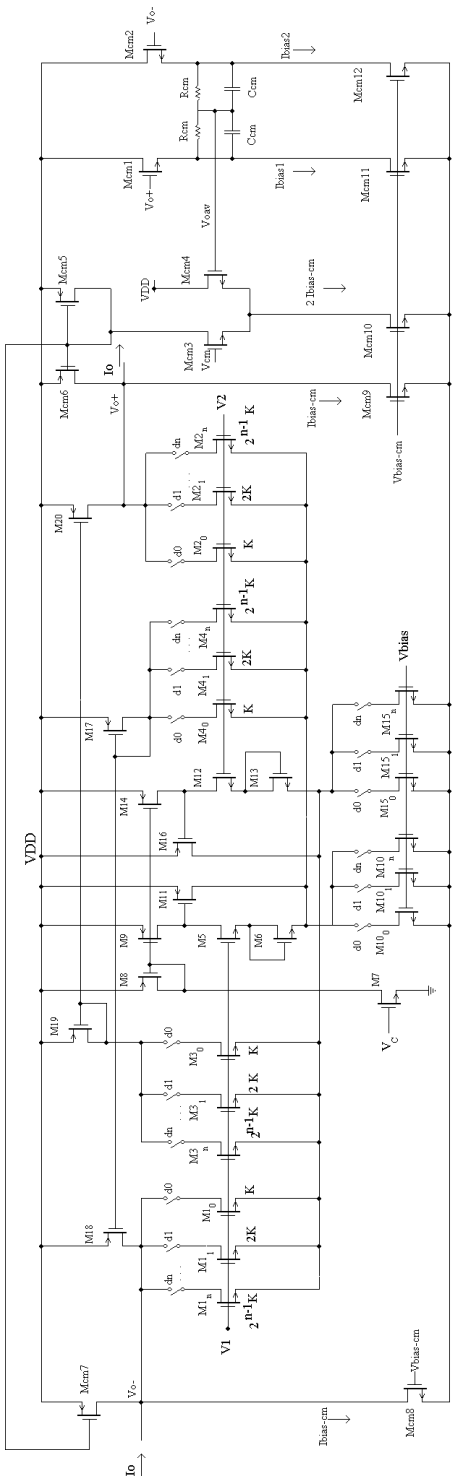

Fig. 5. The CMOS circuit of the DCBOTA with CMFB circuit.

feedback forcing V_{oav} to follow V_{cm}. The operation of the CMFB circuit can be explained as follows. Assuming the ideal case of fully balanced output signals, i.e., $V_{\text{oav}} = 0$. Since V_{oav} and V_{cm} are equal, the tail current (2 Ibias-cm) will be divided equally between Mcm3 and Mcm4. Therefore, a current Ibias-cm will be passed via Mcm5, Mcm6, and Mcm7 to the output nodes and the circuit exhibits the proper biasing even when large differential signals are present. Next consider the case when the magnitude of $V_{\text{o+}}$ is greater than $V_{\text{o-}}$ which results in a positive CM signal at V_{oav}. This voltage will cause the current in Mcm6 and Mcm7 will decrease pulling down the voltages $V_{\text{o+}}$ and $V_{\text{o-}}$ until the CM voltage V_{oav} is brought back to zero. Similarly, in the case of a negative CM signal, the loop will adjust the V_{oav} to be equal V_{cm}.

The performance of the proposed DCBOTA circuit was verified by Spice simulation with supply voltages $\pm 2.5\,\text{V}$ and using $0.35\,\mu\text{m}$ CMOS technology parameters. The output current of the DCBOTA versus the input differential voltage $V_{id} = V_1 - V_2$ with $V_c = 1.35\,\text{V}$ and different control words is shown in Fig. 6. The magnitude responses of the DCBOTA output current are shown in Fig. 7 with 3-dB frequency 146 MHz at 001 control word and 81 MHz at 111 control word. The input referred noise voltage spectral densities for the DCBOTA when terminated by $10\,\text{K}\Omega$ is $80\,\text{nV}/\sqrt{\text{Hz}}$ at 50 MHz and control word 001. The linearity of the DCBOTA was determined by calculating the third-order inter-modulation (IM3) distortion. Two single tone signals of frequency 49 MHz and 51 MHz are applied to the inputs of the DCBOTA. The simulated frequency spectrum of the output is shown in Fig. 8 and the IM3 is around 40 dB. The power supply rejection ratio (PSRR) from positive

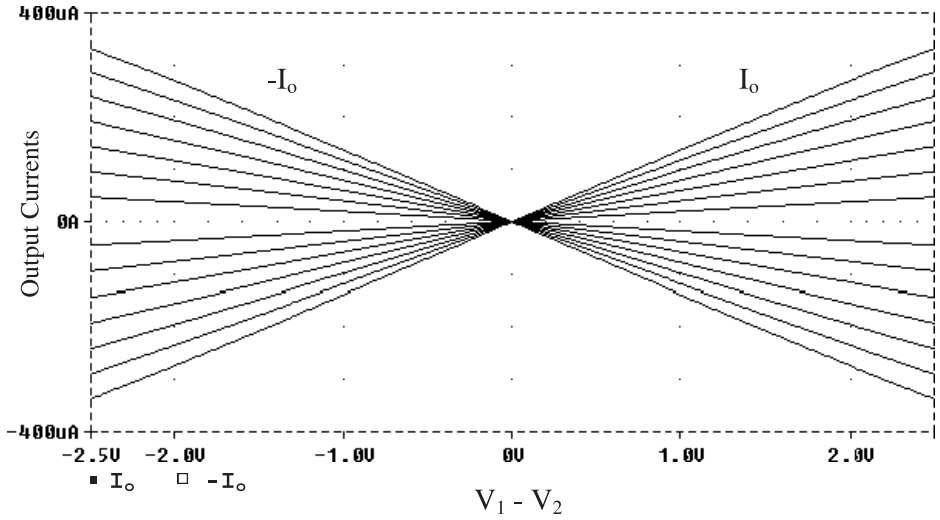

Fig. 6. The DC output currents of the DCBOTA with $V_c = 1.35\,\text{V}$ and different control word.

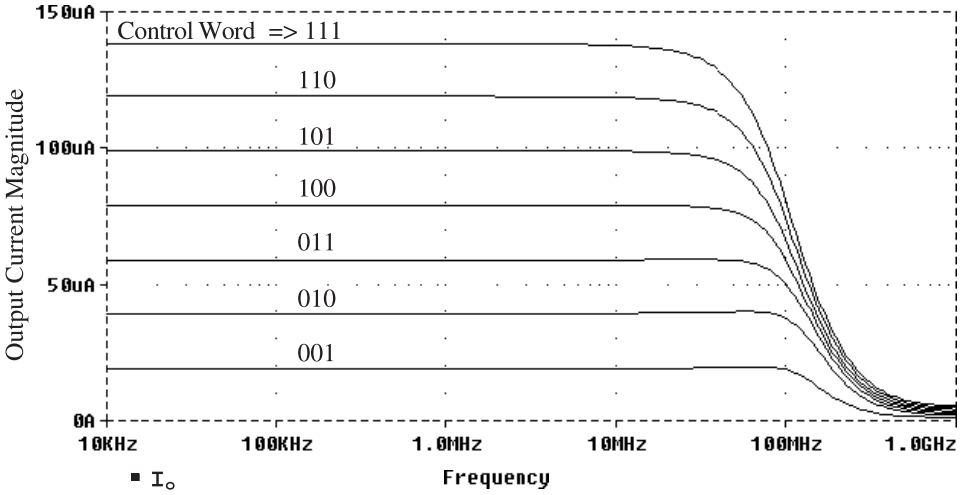

Fig. 7. The magnitude responses of the DCBOTA output currents with $V_c = 1.35\,\mathrm{V}$ and different control word.

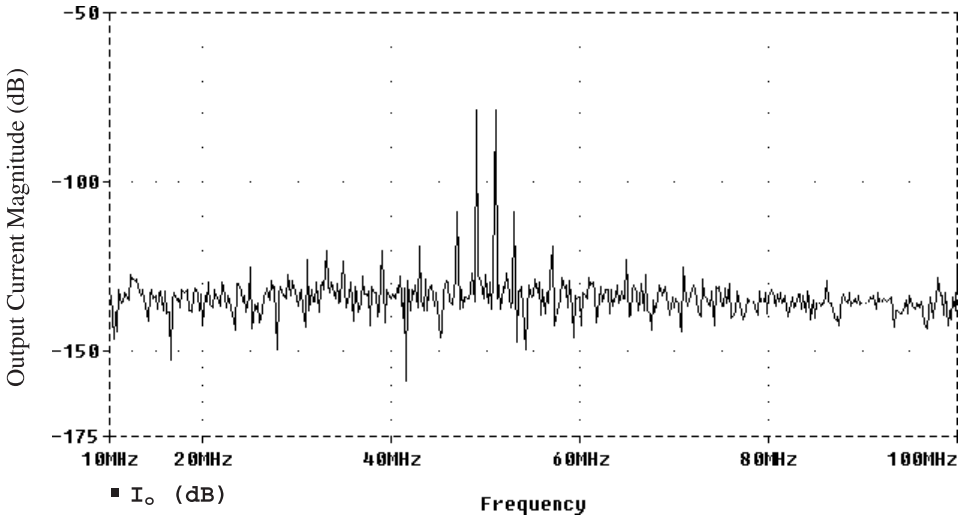

Fig. 8. The simulated IM3 frequency spectrum of the DCBOTA output current with control word 111.

supply is around 124 dB and from the negative supply is around 154 dB. The current consumption is 330 μA at 001 control word and 1.95 mA at 111 control word.

3. DCBOTA Based-Field Programmable Analog Array (FPAA)

FPAA have achieved great benefits in analog circuits and system design. However, the most challenges for the FPAA are high-frequency analog signal processing

applications.[9] Having a balanced operational transconductance amplifier (BOTA) with a digitally programmable transconductance G_m and programmable capacitor array, it is possible to build applications for wide range of frequencies.[1,3–8] A new approach is used to develop FPAA based on a DCBOTA which allows easy adaptability to implement the most analog signal processing blocks. High frequency operation, simple programming methodology and use of standard CMOS fabrication process are the main features of the proposed FPAA.

3.1. *CAB structure*

The CAB is designed such that it can be configured to perform high frequency analog filters. Each CAB consists of four subcells: DCBOTA, a programming shift register, programming capacitor array, and a set of MOSFET switches as shown in Fig. 9. A control word of 15 bits used to program the CAB (DCBOTA: 3 bits, capacitor: 3 bits, switches: 9 bits), also a control voltage V_c controlling the transconductance of the DCBOTA should be specified. The control word is stored in a shift register while the controlling voltage is stored on analog memory module which addressed by a single bit.[10] The chip area of the CAB is $1239\,\mu$m $\times$ $362\,\mu$m using $0.35\,\mu$m CMOS Technology.

The CAB multiplexers have been designed to give internal interconnections flexibility and guaranteed high frequency performance for the CAB. Multiplexers

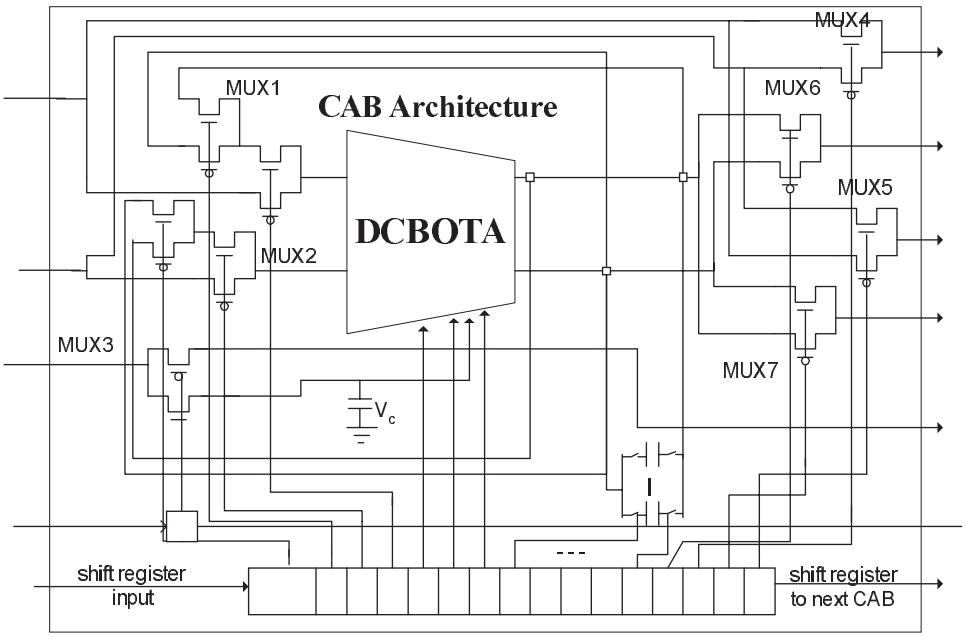

Fig. 9. The proposed configurable analog block (CAB) structure.

are controlled by 9 bits from the internal shift register, as shown in Fig. 9. MUX1 and MUX2 select the inputs of the DCBOTA by sitting control bits equal to "1", the inputs to the CAB block are connected directly to the inputs of DCBOTA, otherwise the feedback path from the output of the DCBOTA is fed to the inputs. MUX3 enables the programming of the control voltage. MUX4 and MUX5 bypass CAB's input to the next neighboring one. MUX6 and MUX7 enable to select one of the DCBOTA outputs to another CAB.

3.2. *Programmable capacitor array*

The programmable capacitor array is shown in Fig. 10. It consists of capacitors C_0, $2C_0$, and $4C_0$ and switches S_1, S_2, and S_3. The capacitor array built of an appropriate number of capacitors connected in parallel. Switches are realized using MOSFETs. When switch S_n, where n is the switch number $\in \{1, 3\}$ is closed the equivalent capacitance to the array could be expressed as $C_{\text{eq}} = C_{\text{array}} + C_{\text{par}}$, where C_{par} is the parasitic capacitance of connections when all switches open and C_{array} is the equivalent capacitance of the array can be expressed as follows:

$$C_{\text{array}} = \sum_{n=1}^{3} S_n C_n \,, \tag{8}$$

where S_n is equal to "1" when switches are closed and equal to "0" when switches are open. The minimum equivalent capacitance equal to 1 pF and the maximum is equal to 7 pF.

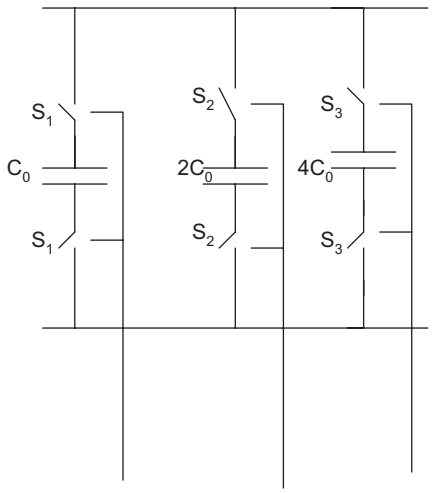

Fig. 10. The programmable capacitor array.

3.3. *FPAA architecture*

The proposed FPAA architecture, Fig. 11, consists of an array of CABs and an interconnect network. Programming shift register are used to program the interconnect network such that each CAB can be connected to all neighboring CABs and to itself in the case of the feedback. One of the problems of the transconductor-based circuits is that the outputs are not buffered, therefore, fully differential buffers[11] are added in the FPAA. The proposed FPAA includes four different differential inputs and three independent fully differential outputs working concurrently.

3.4. *FPAA interconnection*

Connectivity between CAB blocks in the array plays a significant role on the performance of the circuit realized on the FPAA.[12] The FPAA is a regular square array of CABs interconnected, as shown in Fig. 11, with a crossbar structure having horizontal and vertical interconnection lines as shown in Fig. 12. In this cross-bar structure, inputs and output of CAB's can be connected via switches placed in the intersection of the vertical and horizontal lines. With this crossbar structure each CAB could be connected to any neighboring CAB or to the input to the FPAA chip directly. Configuration of this interconnection network could be done by loading design-specific programming stream of bits into FPAA to define their interconnections. Each configuration bit defines the state of an interconnect pass

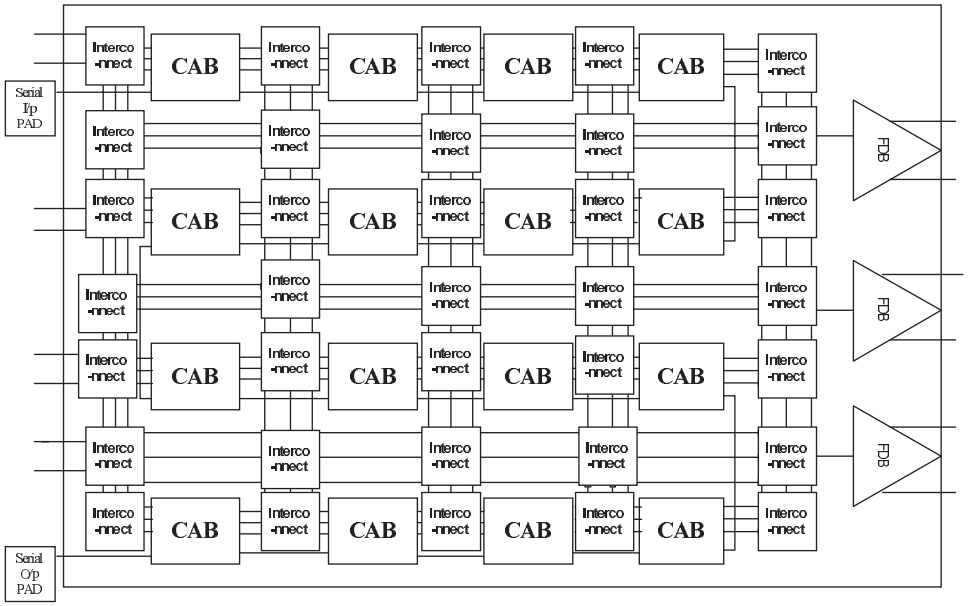

Fig. 11. The proposed FPAA architecture.

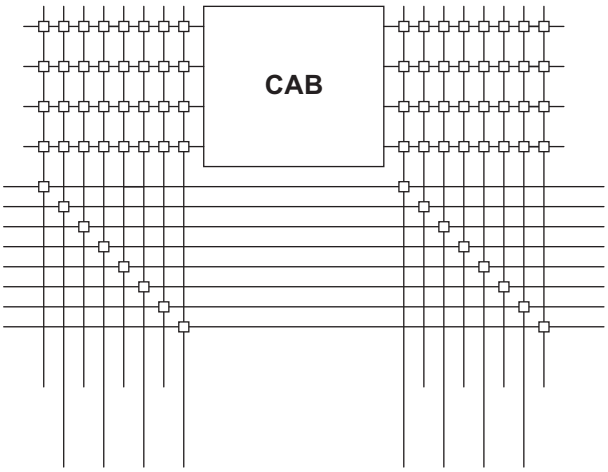

Fig. 12. FPAA interconnection network.

transistor. A global clock line has been added in the FPAA interconnection network for the shift register clock.

The characteristics of the configured function can be programmed through configurable word. The desired connectivity between CABs in an array is determined by the routing word. The digital control words are stored in a single shift register inside the CAB. Shift register inside the CAB could be used to program the DCBOTA, the capacitor array, and the interconnection of the input, output, and feedback switches. All shift registers in CABs are connected in series and collectively acts as a single shift register which can be loaded with the desired programming bit stream through one external pin as indicated in Figs. 9–12.

4. Applications

The proposed DCBOTA can be used to implement the fully differential or fully balanced architecture of any GM-C based circuits.[13] Two design examples are presented in this section to demonstrate the use of the proposed DCBOTA.

4.1. *Digitally controlled variable gain amplifier (DCVGA)*

VGAs are used in many applications to maximize the dynamic range of the overall system.[14,15] A VGA is typically employed in a feedback loop to realize an automatic gain control loop. The use of digital AGC servo loop allows more complex and precise AGC processing using DSP software techniques. It is clear that a digitally controlled VGA would simplify the interface circuitry between the analog and digital parts of the system.[16]

The DCVGA based on the DCBOTA is shown in Fig. 13. The DCVGA consists of two DCBOTA and one fully differential Buffer.[11] The voltage transfer characteristic given by

$$\frac{V_o}{V_i} = \frac{G_1}{G_2} = \frac{V_{C1}(a_0 * 2^0 + a_1 * 2^1 + \cdots + a_n * 2^n)}{V_{C2}(b_0 * 2^0 + b_1 * 2^1 + \cdots + b_n * 2^n)}. \tag{9}$$

The VGA gain is programmed by changing the control words $(a_0, a_1, \ldots, a_n)$ and $(b_0, b_1, \ldots, b_n)$. Figure 14 shows the simulated dc transfer characteristics of the DCVGA. Clearly, the circuit exhibits high linearity for different all possible gain setting. The linearity of the DCVGA was determined by calculating the IM3. Two single tones of frequencies 9 MHz and 11 MHz are applied to the inputs of the

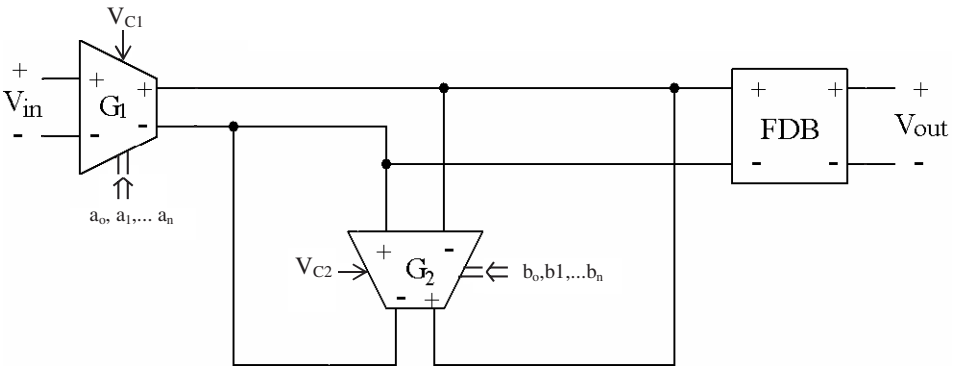

Fig. 13. The DCVGA circuit.

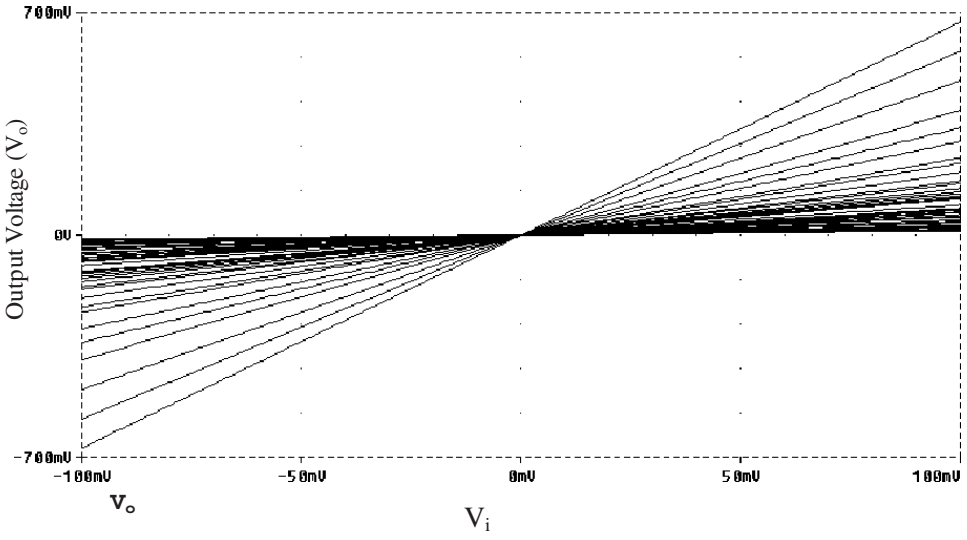

Fig. 14. The simulated DC transfer characteristics of the DCVGA.

DCVGA. The frequency spectrum of the output is shown in Fig. 15. The IM3 is around 50 dB at the maximum gain setting. Figure 16 shows the simulated frequency responses of the DCVGA. It can be seen that the DCVGA based on the ratio between two digitally controlled transconductances enjoys with high bandwidth.

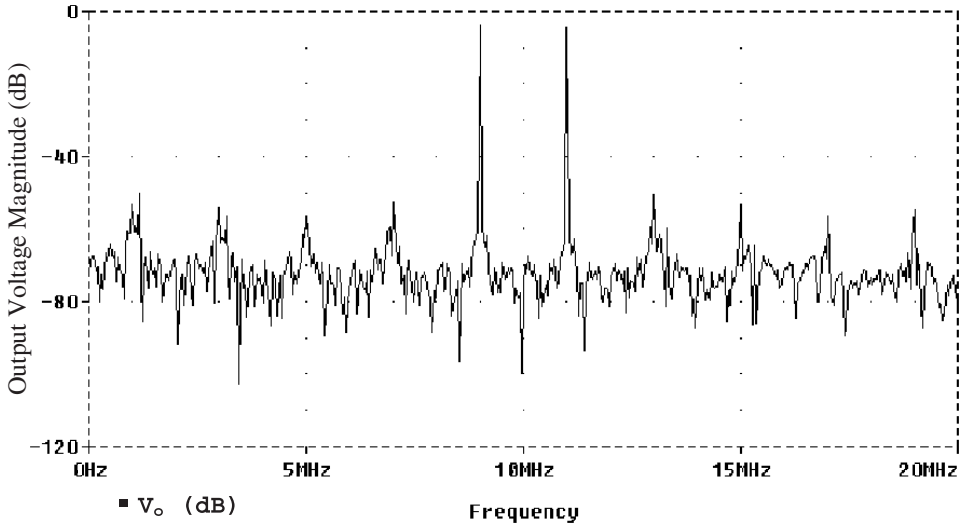

Fig. 15. The simulated IM3 frequency spectrum of the DCVGA output.

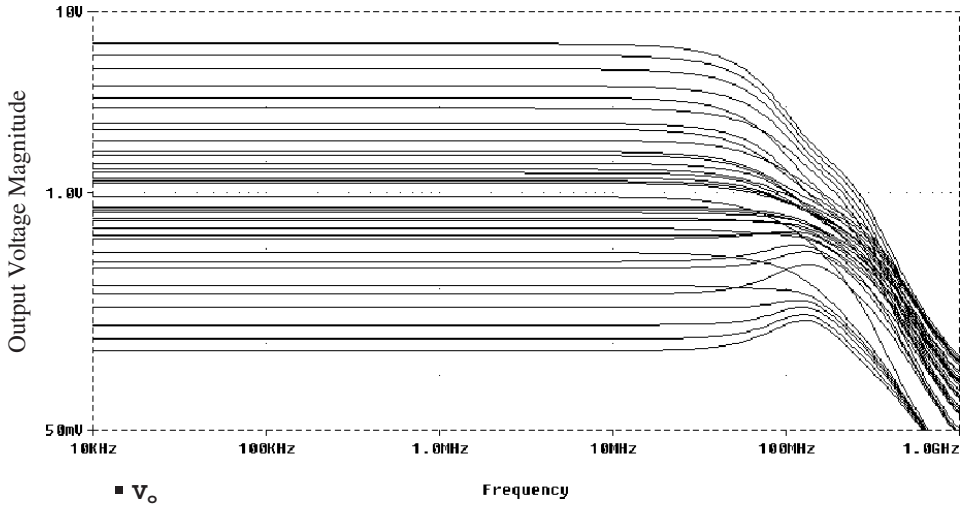

Fig. 16. The simulated frequency responses of the DCVGA.

4.2. *DCBOTA-based LOW pass filter*

Figure 17 represents a filter circuit which realizes second-order fully differential lowpass filter based on the DCBOTA. The circuit includes four DCBOTAs and two capacitors. By direct analysis, the following transfer function is obtained as

$$\frac{V_o}{V_i} = \frac{(G_1G_3/C_1C_2)}{S^2 + S(G/C_1) + (G_1G_2/C_1C_2)}\,. \tag{10}$$

From the above equation, the ω_0, Q and the DC gain H of the filter are given by

$$\omega_0 = \sqrt{\frac{G_1G_2}{C_1C_2}}\,, \quad Q = \frac{1}{G}\sqrt{\frac{G_1G_2C_1}{C_2}}\,, \quad H = \frac{G_3}{G_2}\,. \tag{11}$$

From the above equations, the filter shown in Fig. 17 has the following advantage, the gain of this filter H can be programmed without disturbing ω_0 and Q by tuning G_3, therefore this circuit can be viewed as a lowpass filter with an embedded VGA. The merged filtering and controlled gain results in improving the overall dynamic range, and reduces the required number of amplifier stages of a system. The simulated frequency spectrum of a six-order maximally flat lowpass filter consisting from three cascaded sections of filter shown in Fig. 17 with $G_1 = G_2 = G_3 = G$, and $C_2 = 2\ C_1$ is shown in Fig. 18. The cutoff frequency in tuned from 1 MHz to 7 MHz. Also, the frequency response of this filter for different values of DC gain by programming G_3 is shown in Fig. 19.

5. Conclusion

A high frequency digitally controlled balanced output transconductor (DCBOTA) has been analyzed and simulated. A general CAB consisting of the proposed

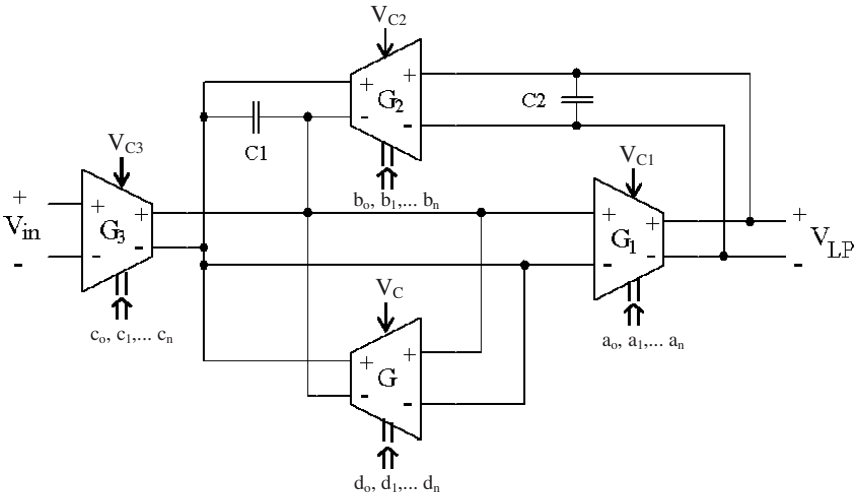

Fig. 17. Second-order fully differential lowpass filter based on the DCBOTA.

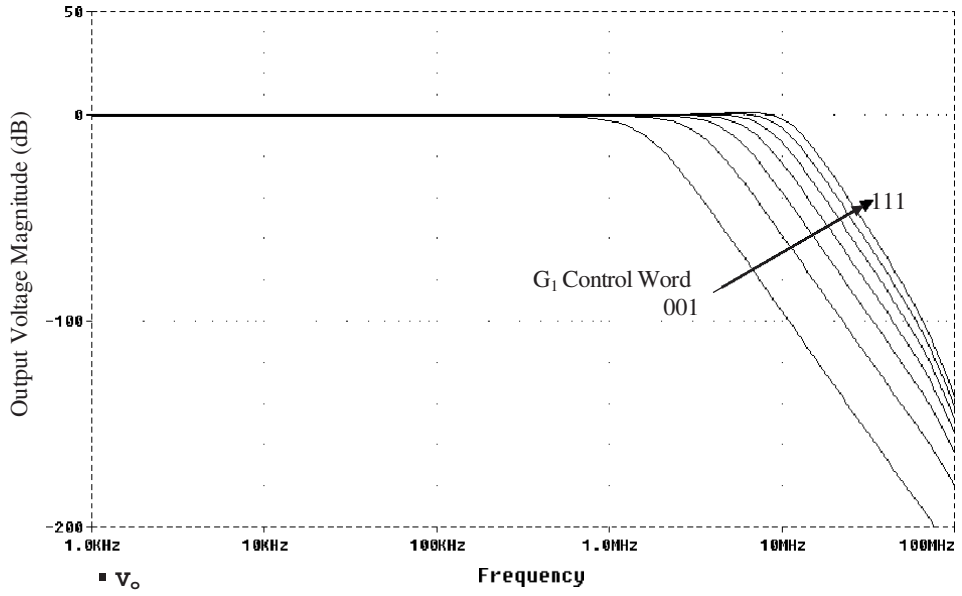

Fig. 18. The frequency response of a six-order maximally flat lowpass filter with tuned cutoff frequency from 1 MHz to 7 MHz.

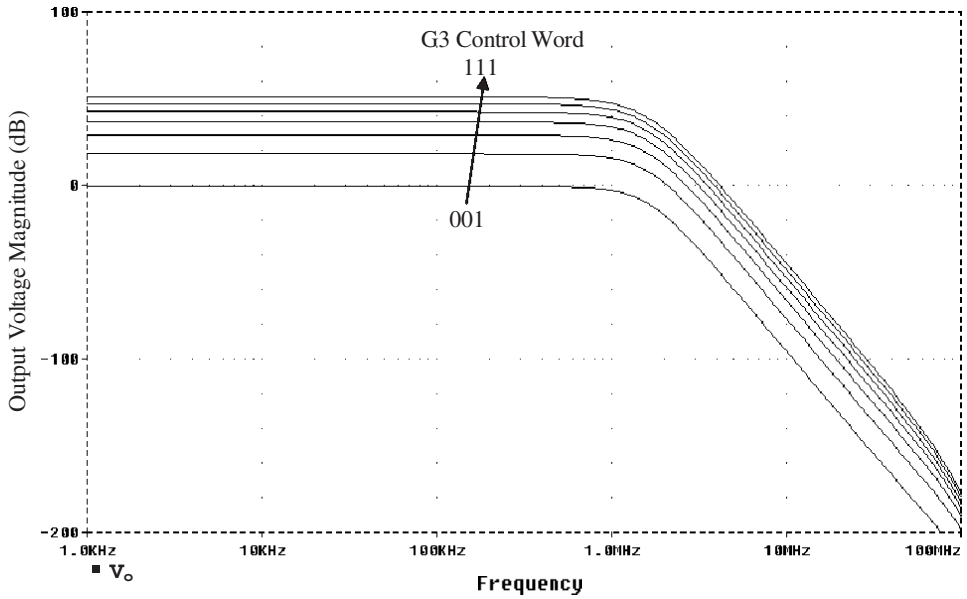

Fig. 19. The frequency response of the six-order filter for different values of DC gain by programming G_3.

DCBOTA, capacitor array and MOS switches have been presented. A collection of the CABs, FDBUFs, and their interconnection to construct a field programmable analog array of 4×4 CABs and 3 FDBUFs has been introduced. Simulations results showed that the DCBOTA has a transconductance tuning range from $20\,\mu$A/V to $140\,\mu$A/V using 3 bits control word, a 3-dB bandwidth larger than 81 MHz, input referred noise voltage spectral densities smaller than $80\,\text{nV}/\sqrt{\text{Hz}}$ at 50 MHz and control word 001, the IM3 of two single tone signals of frequency 49 MHz and 51 MHz is around 40 dB, the PSRR from positive supply is 124 dB and from the negative supply is 154 dB and the current consumption is $330\,\mu$A at 001 control word. Application examples in designing a wide band variable gain amplifier (DCVGA) and six order lowpass filter are also provided. The DCVGA has a gain controllable in the range from -17 dB to 17 dB. The six order lowpass filter has a controllable gain from 0 dB to 51 dB and tunable cutoff frequency from 1 MHz to 7 MHz.

References

1. S. A. Mahmoud and A. M. Soliman, New CMOS programmable balanced output transconductor and application to a mixed mode universal filter suitable for VLSI, *Analog Integrated Circuits and Signal Processing* **19** (1999) 241–254.
2. H. O. Elwan and M. Ismail, A CMOS digitally programmable class AB OTA circuits, *IEEE CAS-II* **47** (2000) 1551–1556.
3. S. A. Mahmoud and A. M. Soliman, A CMOS programmable balanced output transconductor for analog signal processing, *Int. J. Electron.* **82** (1997) 605–620.
4. F. Krummencher and N. Joehl, A 4 MHz CMOS continuous-time filter with on-chip automatic tuning, *IEEE J. Solid State Circuits* **SC23** (1989) 750–758.
5. S. A. Mahmoud and A. M. Soliman, CMOS balanced output transconductor and applications for analog VLSI, *Microelectronics J.* **30** (1999) 29–39.
6. Y. Tsividis, Z. Czarnul and S. C. Fang, MOS transconductors and integrators with high linearity, *Electron. Lett.* **22** (1986) 245–246.
7. S. A. Mahmoud and I. A. Awad, New CMOS balanced output transconductor and application to GM-C biquad filter, *IEEE Int. Symb. Circuits Syst.* **I** (2003) 385–388.
8. V. Gopinathan, Y. Tsividis, K. Tan and P. K. Heste, Design consideration filter for digital video, *IEEE J. Solid State Circuits* **SC25** (1990) 1368–1378.
9. V. C. Guadet and P. G. Gulak, CMOS implementation of a current conveyor-based field programmable analog arrays, *31st. Asilomar Conf. Signals, Systems and Computers*, Vol. II (1998), pp. 1156–1159.
10. J. M. Rabaey, *Digital Integrated Circuits* (Prentice Hall International Inc., 1996).
11. H. Alzaher, H. O. Elwan and M. Ismail, CMOS digitally programmable filter for multi-standard wireless receivers, *Electron. Lett.* **36** (2000) 133–135.
12. S. Brown, R. Francis, J. Rose and Z. Vranesic, *Field Programmable Gate Arrays* (Kluwer Academic Publisher, 1992).
13. S. A. Mahmoud and A. M. Soliman, New CMOS fully differential difference transconductor and application to fully differential filters for VLSI, *Microelectronics J.* **30** (1999) 169–192.

14. H. O. Elwan and M. Ismail, Digitally programmable decibel-linear CMOS VGA for low-power mixed signal applications, *IEEE CAS-II* **47** (2000) 288–298.
15. R. Harjani, A low-power CMOS VGA for 50 Mb/s disk drive read channels, *IEEE CAS-II* **42** (1995) 370–376.
16. H. Alzaher, H. O. Elwan and M. Ismail, A CMOS fully balanced second-generation current conveyor, *IEEE CAS-II* **50** (2003) 278–287.