Digitally Controlled CMOS Balanced Output Transconductor Based on Novel Current-Division Network and Its Applications

Mohammed A. Hashiesh[1], Soliman A. Mahmoud[1], and Ahmed M. Soliman[2]

1. Electrical Engineering Dept., Cairo University, Fayoum Branch, Egypt.
2. Electronics and Communication Eng. Dept., Cairo University, Cairo, Egypt.

Abstract: In this paper, a novel digitally controlled CMOS balanced output transconductor (DCBOTA) is proposed. The digital control of the transconductance of this DCBOTA is achieved using novel current division network (CDN). The proposed DCBOTA operates under low supply voltage of $\pm1.5V$. Application of the DCBOTA is realizing variable gain amplifier VGA and second order active filter. PSPICE simulation confirms the performance of the proposed blocks and its applications.

I. INTRODUCTION

The programmable balanced output transconductor (BOTA) is a useful building block for continuous-time analog signal processing. Based on the BOTA circuit, balanced output integrators, MOS-C filters with balanced outputs and active realization of passive filters with minimum number of BOTA can be built [1,2]. In low voltage applications, there is a limitation on the allowable range of the analog tuning voltage. Hence, in these applications, digital control is more attractive [3]. Another example utilizing digital control is the interface with the digital signal processing unit (DSP) in the modern digital systems. For example the variable gain amplifier (VGA) is used in many applications in order to maximize the dynamic range of the overall system by varying the gain of the VGA. Wireless communication is an example of such systems [4]. In modern wireless systems, all of the baseband signal processing is implemented digitally by a digital signal processor. Hence, a primary requirement of the VGA is to be digitally controlled [5].

In this paper a novel digitally controlled CMOS balanced output transconductor (DCBOTA) is presented. The digital control of the DCBOTA is achieved using novel current division network (CDN) that will be discussed in section III. The traditional approach to implement the CDN is to use the well-known resistive R-2R ladder circuit. For proper operation, all the resistance in the ladder must be matched. This may be very difficult to achieve in practice especially when number of bits increases. Another drawback is that the output resistance of this CDN is small. This means that the output nodes I_{O1} or I_{O2} should be at virtual ground voltages. This prevents the use of this circuit in the applications where the input resistance of the stage next to the CDN is finite. In the DCBOTA, the output current of the CDN is mirrored using MOS transistor which has finite input resistance. Hence, a resistive ladder CDN cannot be used in this application.

A better approach to implement the CDN is to use of MOS ladder circuit [6]. In spite of the advantages of this circuit over its resistor-based counterpart, its structure is similar to the classical resistor based R-2R ladder CDN and still suffers from the drawbacks of it such as finite output resistance, the need of matching all the transistors in the circuit, and the requirement of matched output node voltages of nodes I_{O1} and I_{O2}.

The CDN presented in [3] uses differential-pair current division cell (CDC) technique to divide the input current of the CDC into two equal divisions if the gates of the two MOS transistors constructing the differential pair are kept under the same voltage level. For proper operation, the n-bits CDN requires (n+1) biasing voltages to be connected to the gates of the differential pairs of the n-CDCs. To generate those biasing voltages, a very complex design is required. The number of control bits is limited by those biasing voltages which are limited by the power supply range.

As in the differential-based CDN, the proposed CDN has very high output resistance since the output currents are drown from the drain of the transistors (as will be discussed later). Hence, no need for virtual ground nodes. Consequently, the aspect ratio of the transistors can be chosen arbitrary to achieve the required current level without putting stringent requirement on the stage next to the CDN. Besides, only the transistors inside each CDC are required to be matched rather than matching all the transistor in the entire CDN. Hence, the matching-requirements are relaxed. Since the transistor are assumed to operate in the saturation region, higher current drive capability is expected than in the case of the MOS ladder for the same aspect ratios of transistors. Moreover, the proposed CDN has no limitation on the number of the control bits as in the case of the differential-based CDN. And no need to external biasing voltages.

II. THE PROPOSED DCBOTA

The CMOS realization of the proposed DCBOTA circuit is shown in Fig. 1(b). It consists of a basic four matched-transistors M_1-M_4 drive two similar CDNs. The output currents of the two CDNs are transferred to output nodes by the rest of the circuit M_5-M_{14} to get the two balanced output currents of the DCBOTA. As will be discussed in the following section, the value of the input current to the CDN is divided between two complementary output currents depending on the digitally controlled parameter α ($I_{O1}=\alpha I_I$, and $I_{O2}=(1-\alpha)I_I$). The two current division blocks (CDN$_1$ and CDN$_2$) in Fig. 1(b) are controlled by the same control word. Hence, the output current of the DCBOTA can be driven as follows:

The matched transistors M_1-M_4 are the basic transistors, and their gate voltages are the input voltages to the transconductor. All transistors are assumed to be operating in saturation region with their sources connected to their substrate/bulk. The MOS drain current in the saturation region is given by:

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \qquad (1)$$

Where $K=\mu_n C_{ox}(W/L)$; (W/L) is the transistor aspect ratio, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, and V_T is the threshold voltage (assumed the same for all MOS transistors).

From Fig. 1(b),

$$I_{OA} = I_1 + I_4 \qquad (2)$$

$$I_{OB} = I_2 + I_3 \qquad (3)$$

The first current-division of CDN_1 and CDN_2 is αI_{OA} and αI_{OB} respectively. The remaining transistors M_5-M_{14} perform current transfer for those two currents to the output port of the transconductor, hence, the output current of the transconductor I_o is given by:

$$I_O = \alpha(I_{OA} - I_{OB}) \qquad (4)$$

Using equations (1)-(4), the transconductor output current is given by:

$$I_O = \alpha K(V_C - V_{SS})(V_1 - V_2) \qquad (5)$$

Therefore, the proposed DCBOTA circuit shown in Fig. 1 operates as a digitally controlled balanced output transconductor with programmable transconductance G which is controlled by the digitally controlled parameter α and is given by:
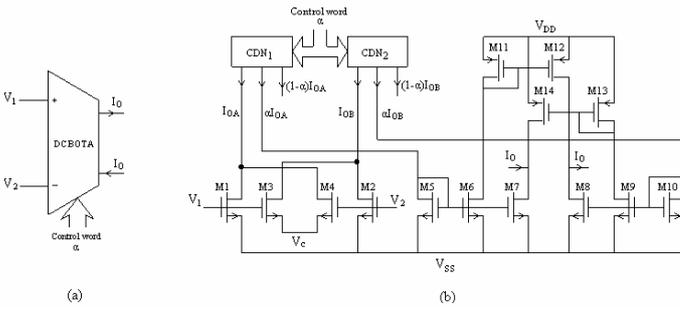
$$G = \alpha K(V_C - V_{SS}) \qquad (6)$$

Fig. 1: Proposed DCBOTA (a) Symbol (b) CMOS Realization

Note that the tuning of the DCBOTA is achieved using the digitally controlled parameter α where $\alpha \leq 1$; i.e. the maximum transconductance value is achieved at $\alpha=1$ and is equal to $K(V_C-V_{SS})$ where V_C and V_{SS} are DC control voltage and the negative supply voltage respectively. The operation of the CDN block is described in the following section.

III. THE PROPOSED CDN

The block diagram of the proposed CDN is shown in Fig. 2. It consists of n current division cells (CDCs). According to the current division principle, each CDC of this network has three output currents. The output currents of the current division cell number i CDC_i are I_{O1i}, I_{O2i}, and I_{O3i} whose relations to the input current of this cell (I_{Ii}) are expressed as follow:

$$I_{O1i} = a_i \frac{I_{Ii}}{2} \qquad (7)$$

$$I_{O2i} = \bar{a}_i \frac{I_{Ii}}{2} \qquad (8)$$

$$I_{O3i} = \frac{I_{Ii}}{2} \qquad (9)$$

Where a_i is the digital control bit of this cell. As shown from Fig. 2, I_{O3i} of the CDC_i is used as the input current of the next stage $I_{I(i-1)}$ and I_{O30} has inverted direction, as will be discussed later, and is added to I_{O2}. Therefore, the two output currents of the CDN are given by:

$$I_{O1} = \sum_{i=0}^{i=n-1} I_{O1i} = \frac{1}{2^n}\left(\sum_{i=0}^{i=n-1} 2^i a_i\right)I_I \qquad (10)$$

$$I_{O2} = I_{O30} + \sum_{i=0}^{i=n-1} I_{O2i} = \frac{1}{2^n}\left(1 + \sum_{i=0}^{i=n-1} 2^i \bar{a}_i\right)I_I \qquad (11)$$

$$\alpha = \frac{I_{O1}}{I_I} = \frac{1}{2^n}\left(\sum_{i=0}^{i=n-1} 2^i a_i\right) \qquad (12)$$

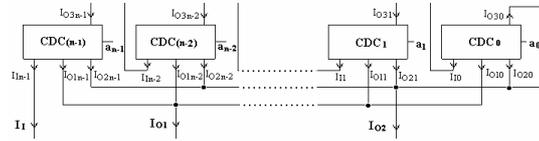Hence, the current gain of the proposed CDN is digitally controlled.
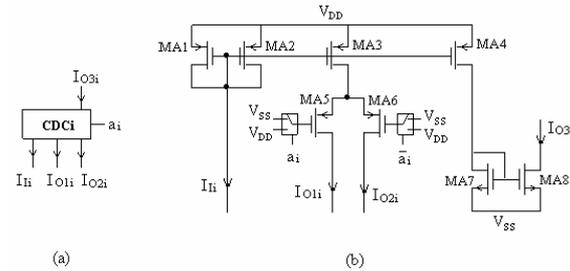

Fig. 2: Proposed CDN Block Diagram

Fig. 3: Proposed CDC (a) Symbol (b) CMOS Realization

The proposed CDC is shown in Fig. 3. For the matched transistors M_{A1}-M_{A4}, the input current of the CDC$_i$ (I_{Ii}) is divided between M_{A1} and M_{A2} then this value is transferred to both M_{A3} and M_{A4} by the current mirror effect. Only one transistor of M_{A5} or M_{A6} is on at a time due the value the digital control bit a_i. Hence, the current of $I_{Ii}/2$ which flowing through M_{A3} is either switched to I_{O1i} or I_{O2i} as equations (7) and (8) indicate. The current flowing through M_{A4}, which also equal to $I_{Ii}/2$, is transferred to I_{O3i} through M_{A7} and M_{A8} as stated in equation (9). For the last stage CDC_0, no need to M_{A7} and M_{A8} and the current I_{O30} is simply equal to the current of M_{A4}.

The proposed DCBOTA circuit has been simulated using PSPICE simulation with 0.5μm CMOS parameters (level3). The power supply voltages V_{DD} and V_{SS} are balanced (1.5V and -1.5V) respectively. The aspect ratios of the transistor are given in Table 1 and n = 8 bits. The DC control voltage (V_C) is –1.1 V. The two balanced output currents of the DCBOTA is shown in Fig. 4 when driving $R_{L+}=R_{L-}=8K\Omega$ and the differential input voltage is swept from –1 to 1V for different values of the digitally controlled

parameter α ranging from 0 to 1 in 0.125 step. Fig. 5 shows the frequency response of the output current when $R_{L+}=R_{L-}=8K\Omega$ and $\alpha = 1$ from which it is seen that the bandwidth is approximately equal to 21 MHz

Table 1: Aspect Ratios of The Proposed DCBOTA

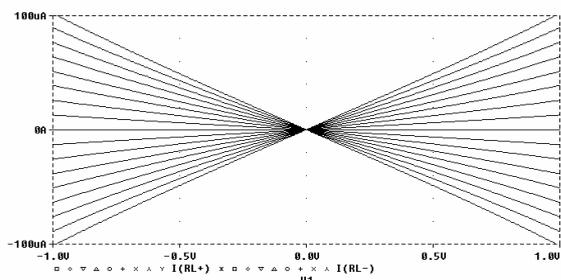| Transistor	Aspect Ratio [μm/μm]
$M_1, M_2, M_3, M_4.$	22/6
$M_5, M_6, M_7, M_8, M_9, M_{10}.$	80/2
$M_{11}, M_{12}, M_{13}, M_{14}.$	160/2
$M_{A1}, M_{A2}, M_{A3}, M_{A4}, M_{A5}, M_{A6}, M_{A7}$	100/1

Fig. 4: DC Transfer Characteristics of The Proposed DCBOTA
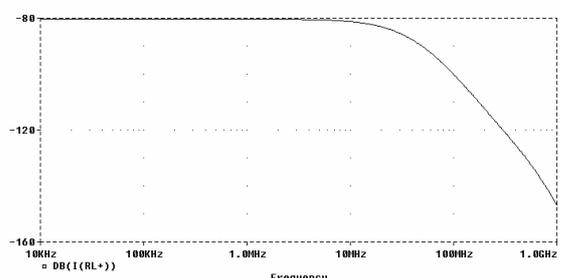

Fig. 5: Frequency Response of The Output Current of The Proposed DCBOTA

IV. DIGITALLY PROGRAMMABLE FULLY DIFFERENTIAL VGA

Variable gain amplifiers (VGA) are employed in many applications in order to maximize the dynamic range of the overall system. For example; in any portable communication system, the VGA is employed in feedback loop to realize an automatic gain control loop (AGC)[7]. Receiver portability implies that the receiver may be very close to the transmitter and thus receiving strong signal, or far away receiving weak signal. The function of the AGC loop is to automatically adjust the gain of the receiver path so that the signal processed by the base band circuitry appears to be of constant level regardless of the actual signal size received at the antenna. In modern wireless systems, all of the baseband signal processing is implemented digitally by a digital signal processor. Hence, a primary requirement of the VGA is to be digitally controlled [5].

The digitally-controlled fully-differential VGA can be implemented using DCBOTA as shown in Fig. 6. For Fig. 6(a), The VGA circuit consists of DCBOTA Transconductor driving load resistance R_L. The DCBOTA has transconductance G given by equation (6). Thus, the fully differential output voltage $(V_{O1}-V_{O2})$ can be driven as follows:

$$(V_{O1} - V_{O2}) = 2GR_L(V_1 - V_2) \qquad (13)$$

Where G is controlled by α, α is the digital control parameter given by equation (12).

Hence the number of the control bits is 8 bits, and from equation (12), if the value of $2GR_L/\alpha$ is designed to be equal 2^8, The above configuration of the VGA can be operated with dB-linear gain if α has only one bit of the 8 control bits activated at a time as shown in Table 2. Thus could be obtained using simple 3X8 decoder to reduce the required control word to only 3 bits. The minimum gain is 0 dB and is obtained when the least significant bit is active. The maximum gain is 42 dB when the most significant bit is active. Hence, the gain step is 6 dB that appear to be quit large. To realize dB-linear VGA with wide control range and fine step, two DCBOTAs are cascaded as shown in Fig. 6(b). $DCBOTA_2$ and its load R_{L2} are designed as in the previous configuration to operate with 6 dB coarse step controlled by α_2 while $DCBOTA_1$ and R_{L1} are designed to operate with the required fine step with the appropriate decoder, the VGA is thus operating in a fine and coarse arrangement.

The differential gain of the proposed VGA in Fig. 6(a) is sown in Fig. 7 in dBs versus the differential input voltage when the gain is scanned from 0 dB to 30 dB with gain step of 6 dB, where the DCBOTA is designed as in Table 1 and $R_L=1.25M\Omega$.
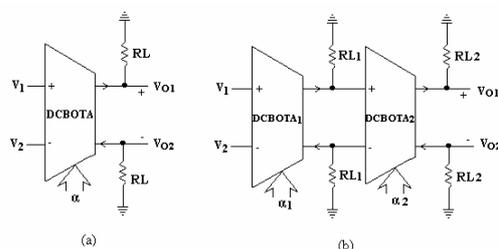

(a)   (b)

Fig. 6: Proposed VGA (a) First Configuration (b) Second Configuration
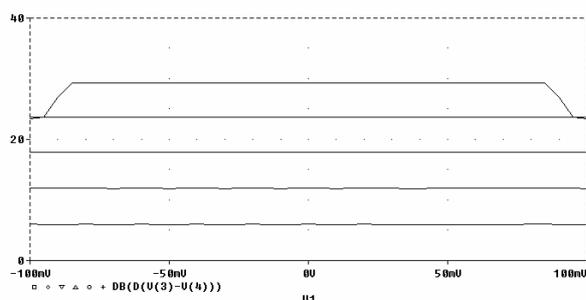

Fig. 7: dB Gain of The Proposed VGA at Gain Step = 6 dB

V. DIGITALLY PROGRAMMABLE FILTER

The active filter presented in [2] can be implemented using DCBOTA to handle the advantages of the digital control and simply interface the DSP units in the modern digital systems. Fig. 8 represents this filter circuit which includes four DCBOTAs and two grounded capacitors and realizes second-order lowpass, bandpass, allpass and notch responses. The lowpass and bandpass exist in the voltage and current modes; however, the allpass and notch outputs exist only in current mode and obtained by combining I_{BP} and I_i (I_i is the output current of the transconductor G_3). By direct analysis, the following transfer functions are obtained:

$$\frac{V_{LP}}{V_i} = -\frac{G_1 G_3 / C_1 C_2}{D(S)}, \quad \frac{I_{LP}}{V_i} = -\frac{G_1 G_2 G_3 / C_1 C_2}{D(S)} \quad (14)$$

$$\frac{V_{BP}}{V_i} = \frac{SG_3 / C_1}{D(S)}, \quad \frac{I_{BP}}{V_i} = \frac{SG_1 G_3 / C_1}{D(S)} \quad (15)$$

Where,

$$D(S) = S^2 + \frac{G}{C_1}S + \frac{G_1 G_2}{C_1 C_2} \quad (16)$$

From the above equation, the w_o and Q of the filter are given by:

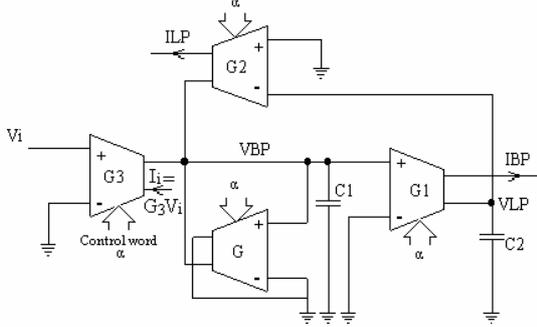$$w_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}}, \qquad Q = \frac{1}{G}\sqrt{\frac{G_1 G_2 C_1}{C_2}} \quad (17)$$

Fig. 8: DCBOTA-C Active Filter

The circuit of Fig. 8 has been simulated using PSPICE simulation with $C_1=C_2=7pF$, and $G_1=G_2=G_3=20G=\alpha K(V_C-V_{SS})$ $\mu A/V^{-1}$ to obtain bandpass filter with $Q=20$, and digitally tunable f_o. The frequency response of that filter is shown Fig. 9 for different values of the digital control parameter α. Fig. 10 shows the simulation results for the same circuit with $C_1=C_2=7pF$, and $G_1=G_2=G_3=0.707G$ $=\alpha K(V_C-V_{SS})$ $\mu A/V^{-1}$ to obtain a maximally flat low pass response for a DC gain of 1 and with digitally tunable f_o for different values of the digital control parameter α.
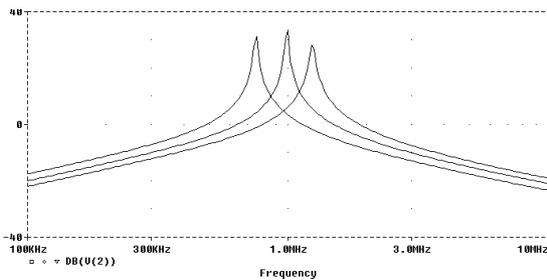

Fig. 9: The Magnitude Response of the Voltage-Mode Bandpass Output
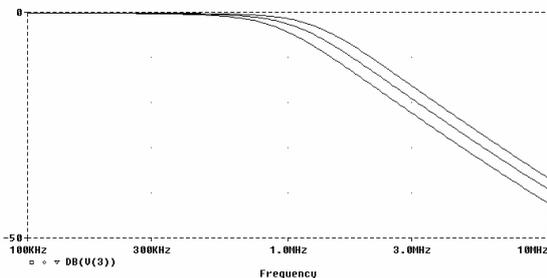

Fig. 10: The Magnitude Response of the Voltage-Mode Lowpass Output

Table 2: Digital Control Word For The Proposed dB-Linear VGA

Digital Control Word								Gain
a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	dB
0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	0	6
0	0	0	0	0	1	0	0	12
0	0	0	0	1	0	0	0	18
0	0	0	1	0	0	0	0	24
0	0	1	0	0	0	0	0	30
0	1	0	0	0	0	0	0	36
1	0	0	0	0	0	0	0	42

VI. CONCLUSION

In this paper, a novel digitally controlled CMOS balanced output transconductor DCBOTA has been proposed. Novel current division network CDN has been used to provide the digital control of the transconductance of this transconductor that simply is a four-transistor cell. Application of the DCBOTA is realizing dB-linear variable gain amplifier VGA and second order active filter. The proposed DCBOTA and its applications have been confirmed using PSPICE simulation.

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