Low Voltage Fully Differential CMOS Current Feedback Operational Amplifier

Soliman. A. Mahmoud

Electronics and Communications Engineering Department, Cairo University, Fayoum Campus, Fayoum, Egypt.

Abstract- This paper presents a new CMOS Fully differential current feedback operational amplifier (FDCFOA). The proposed CMOS realization of the FDCFOA is based on a novel class AB fully differential buffer circuit. Besides the proposed FDCFOA circuit is operating at supply voltages of ±1.5 V, it has a total standby current of 400μA. The applications of the FDCFOA to realize variable gain amplifier, fully differential integrator, and fourth order fully differential maximally flat low pass filter are given. The fourth order filter provides 8dB gain and a bandwidth of 4.3MHz to accommodate the wideband CDMA standard. The proposed FDCFOA and its applications are simulated using CMOS 0.35μm technology.

I. INTRODUCTION

In recent years, fully differential circuit configurations have been widely used in high-frequency analog signal applications like switched capacitor filters [1] and multi-standard wireless receivers [2]. As compared to their single-ended counterparts, they have higher rejection capabilities to clock-feed-through, charge injection errors and power–supply noises, larger output dynamic range, higher design flexibility, and reduced harmonic distortion. In this paper, a new fully differential CMOS current feedback amplifier (FDCFOA) is proposed. The proposed CMOS realization of the FDCFOA is based on a novel class AB fully differential buffer circuit. The FDCFOA has the advantages of the single ended CFOA beside the advantages of the fully differential signal processing. The FDCFOA has many useful applications like the single ended CFOA [3-13].

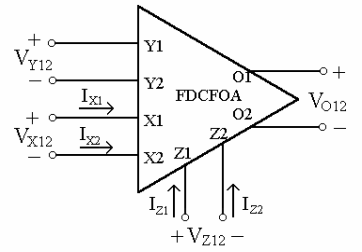

Fig. 1 The symbol of the FDCFOA.

The FDCFOA is basically a four fully differential terminals device as shown in Fig.1. The Y_{12} terminal is a high impedance terminal and the X_{12} terminal is low impedance one. The voltage applied to the terminal Y_{12} is conveyed to the X_{12} terminal ($V_{Y12}=V_{X12}$), while the currents applied to the X_{12} terminal is mirrored to Z_{12} terminal ($I_{x1}=I_{z1}$, $I_{x2}=I_{z2}$). The Z_{12} terminal is a high impedance output node suitable for current output. The voltage developed at the Z_{12} terminal is buffered by a unity gain fully differential voltage buffer to the output terminal ($V_{Z12}=V_{O12}$). The block diagram of the FDCFOA is shown in Fig.2 The input stage FDB1 is a unity gain fully differential buffer forcing V_{X12} to follow V_{Y12}. The currents in the X_{12} terminal is transferred to the high impedance node Z_{12} by the current mirrors. The output voltage is obtained by a second fully differential unity gain buffer FDB2. Therefore, the structure of the FDCFOA is based on the two FDB and current mirrors.

The paper is organized as follows. In section II, the realization of FDCFOA is presented. In section III, applications of the FDCFOA in realizing fully differential integrator, fourth order fully differential maximally flat low pass filter consisting from two cascaded biquad sections are given. Spice simulations of the proposed FDCFOA and its applications using CMOS 0.35 μ m technology are also given.

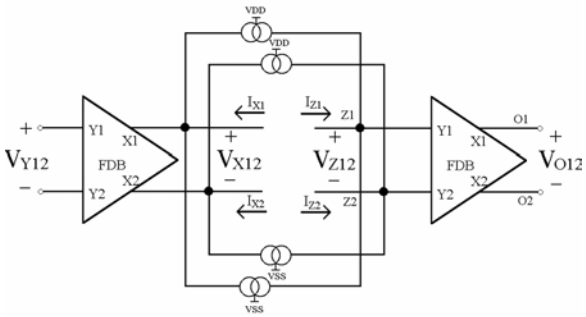

Fig. 2 The block diagram of the FDCFOA.

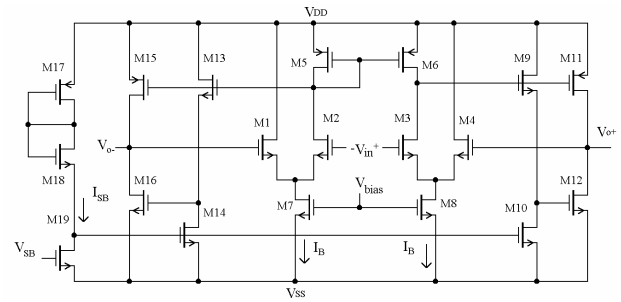

Fig. 3 The CMOS circuit of the FDB.

II. CMOS REALIZATION OF THE FDCFOA

The structure of the proposed FDCFOA is based on the proposed class AB fully

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differential buffer (FDB) circuit shown in Fig.3. The proposed FDB is consisting of two matched differential pairs (M1, M2) and (M3, M4), matched biasing current source transistors (M5, M6), (M7, M8) and two class AB output stages (M9 to M12 and M13 to M16) and the biasing of the output stages (M17 to M19). The differential input is applied to the two high impedance terminals of the NMOS transistors M2 and M3.

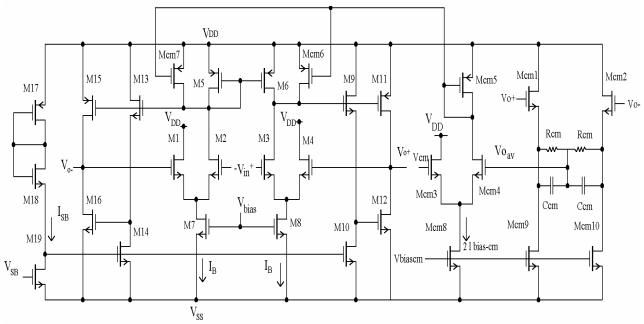

Fig. 4 The CMOS circuit of the FDB with the CMFB circuit.

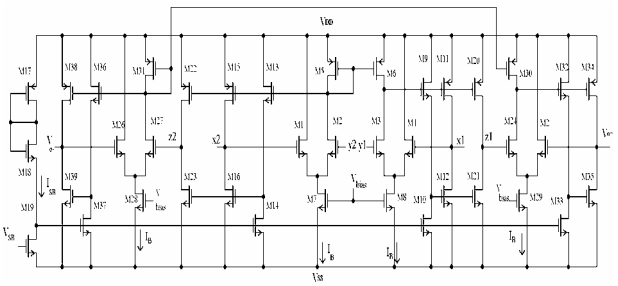

Fig. 5 The CMOS circuit of the FDCFOA.

As a result the tail current transistors M7 and M8 carry equal bias current I_B , Therefore:

$$I_{M1} + I_{M2} = I_{M3} + I_{M4} \quad (1)$$

And by the current mirror action of transistors (M5 and M6):

$$I_{M2} = I_{M3} \quad (2)$$

From the above equations it follows that $I_{M1} = I_{M4}$.The matched differential pair transistors carry equal differential and common mode current values. Therefore,

$$V_{o+} - V_{o-} = V_{i+} - V_{i-} \quad (3)$$

To maintain a good current drive capability with low output impedance outputs, class AB output stages are used. Transistors (M11, M12) and (M15, M16) form the push pull output stage transistors. The level shift circuits formed by (M9, M10) and (M13, M14) are used to realize a controlled floating voltage sources that controls the standby current through the output stage transistors. The current is adjusted by the biasing circuit formed of M17, M18, and M19. The standby power consumption of the overall circuit for dual power supply is given by :

$$P_{SB}=2V_{DD}(3\,I_{SB} + 2\,I_B + K_9(V_{DD} - V_{Tn} + V_{Tp})^2) \quad (4)$$

The last term in the above equation is the current through the level shift transistors (M9, M10) and (M13, M14). This current can be kept small by choosing a small aspect ratio for (M9, M10) and (M13, M14). The class AB output stage enables the circuit to derive heavy resistive and capacitive load with low standby power dissipation and no slewing. It is worth mentioning that smaller miller compensation capacitors can be connected between the gate and drain of transistors M11 and M15 to ensure good transient response under all load conditions.

To prevent the drift in the output common mode (CM) voltage, a common mode feedback (CMFB) circuit is needed. It determines the output CM voltage and controls it to a specified value V_{cm} (usually mid-rail) even with the presence of a large differential signals. When dual power supplies are used V_{cm} is set to zero Volt. The CMFB circuit consists of transistors Mcm1 to Mcm10 as shown in Fig. 4 in addition to two resistors (R_{cm}) and two capacitors (C_{cm}) which are used to control the CM voltage of the outputs (V_{o+} and V_{o-}). Transistors Mcm1 and Mcm2 are employed to isolate the CMFB circuit from the basic circuit. This is essential to make the input current of the CMFB circuit equal to zero. The CMFB circuit generates the CM voltage of the output signals at node V_{oav} via the two equal resistors (R_{cm}). This voltage is then compared to V_{cm} using differential amplifier Mcm3 and Mcm4 with negative feedback forcing V_{oav} to follow V_{cm}.

The operation of the CMFB circuit can be explained as follows. Assuming the ideal case of fully balanced output signals; i. e., V_{oav} =0. Since V_{oav} and V_{cm} are equal, the tail current (I_B/2) will be divided equally between Mcm3 and Mcm4. Therefore, a current I_B/4 will be passed via Mcm5, Mcm6 Mcm7 to the output nodes and the circuit exhibits the proper biasing even when large differential signals are present. Next consider the case when the magnitude of V_{o+} is greater than V_{o-} which results in a positive CM signal at V_{oav}. This voltage will cause the current in Mcm6 and Mcm7 will increase pulling down the voltages V_{o+} and V_{o-} until the CM voltage V_{oav} is brought back to zero. Similarly, in the case of a negative CM signal, the loop will adjust the V_{oav} to be equal V_{cm}.
From the block diagram of FDCFOA in Fig.2, the overall CMOS circuit of the FDCFOA without the common mode feedback circuit is shown in Fig.5.

The performance of the proposed FDCFOA circuit was verified by Spice simulation with supply voltages ±1.5V and using 0.35μm CMOS technology parameters. Fig.6 shows the current at the Z_{12} terminal when X_{12} terminal current is scanned from -100μA to 100μA while the Y_{12} and Z_{12} terminals are

grounded. Fig.7 shows the X_{12} terminal offset variation versus I_{X12} when the Y terminal is grounded.

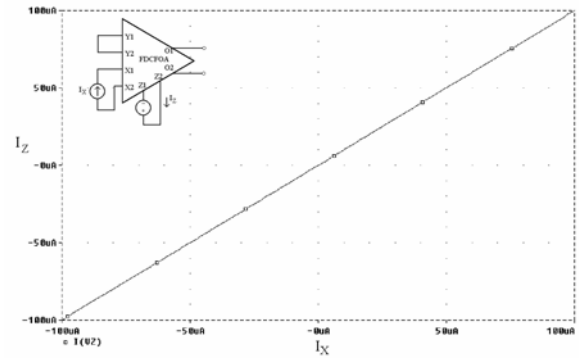

Fig. 6 The Z_{12} terminal current

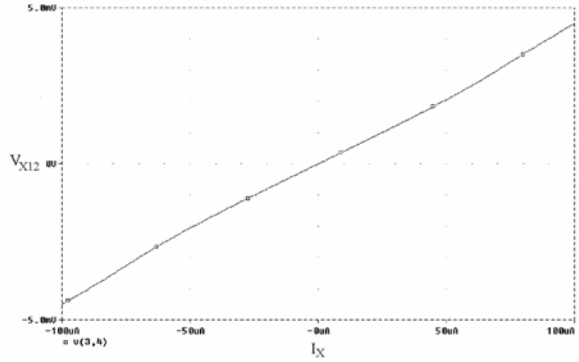

Fig. 7 The X_{12} terminal offset voltage.

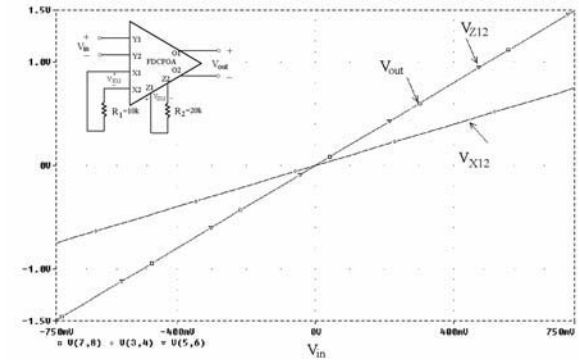

Fig. 8 The voltage swing at the X_{12}, Z_{12} and the O_{12} terminal of the FDCFOA based amplifier.

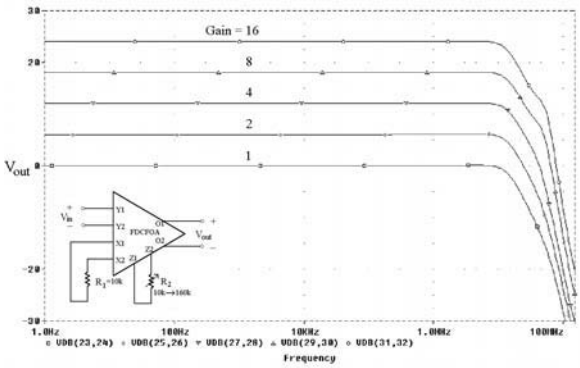

Fig. 9 The frequency response of the FDCFOA based variable gain amplifier.

The X_{12} terminal output resistance is less than 50Ω Fig.8 shows the voltage swing at the X_{12}, Z_{12} and the O_{12} terminals when used to realize a voltage amplifier of gain two. The frequency response of the FDCFOA based variable gain amplifier (VGA) of gain 1,2,4,8,16 is shown in Fig.9. It is clear from Fig.9 that the VGA based on the FDCFOA experience no loss of bandwidth of approximately 20MHz when the gain is increased.

III. Applications

The proposed FDCFOA can be used to implement the fully differential or fully balanced architecture of any CFOA based circuits. Two design examples are presented in this section to demonstrate the use of the proposed FDCFOA.

A. Fully Differential Integrator

The fully differential integrator is a basic building block in realizing continuous time filters [3,4,6]. Fg.10 shows the FDCFOA based fully differential integrator. The output voltage of the integrator is taken from the buffered O_{12} terminal and is given by:

$$V_o = \frac{1}{SCR} V_I \qquad (5)$$

PSpice simulation results for the FDCFOA based fully differential integrator are shown in Fig.11 with a square wave input of 1 V peak to peak amplitude and a frequency of 100KHz, where R =10KΩ and C= 250 pF.

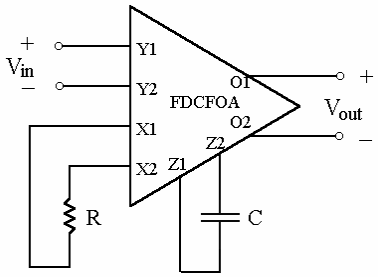

Fig. 10 The fully differential integrator.

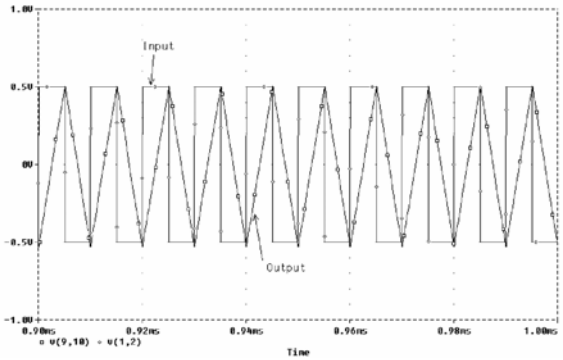

Fig. 11 The output of the integrator along with the square wave input signal.

B. FDCFOA- based LOW Pass Filter

The FDCFOA is used to implement a fully differential version of the Sallen–Key filter. The filter

section shown in Fig.12 represent a filter circuit which realizes second order fully differential lowpass filter based on a single FDCFOA. By direct analysis, the following transfer function is obtained as:

$$\frac{V_o}{V_I} = \frac{\frac{K}{R_1R_2C_1C_2}}{S^2 + S[\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1-K}{R_2C_2}] + \frac{1}{R_1R_2C_1C_2}} \quad (6)$$

From the above equation, for equal R and equal C design, the ω_o, Q and the DC gain H of the filter are given by:

$$\omega_o = \frac{1}{RC}, \quad Q = \frac{1}{3-K}, \; H = K \quad (7)$$

The simulated frequency spectrum of a fourth order maximally flat lowpass filter consisting from two cascaded sections of filter shown in Fig.12 is shown in Fig.12. The cutoff frequency. The fourth order filter provides 8dB gain and a bandwidth of 4.3 MHz to accommodate the wideband CDMA standard.

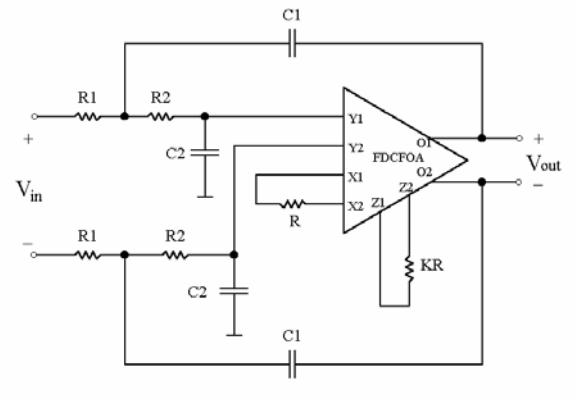

Fig. 12 The fully differential filter section based on the proposed FDCFOA.

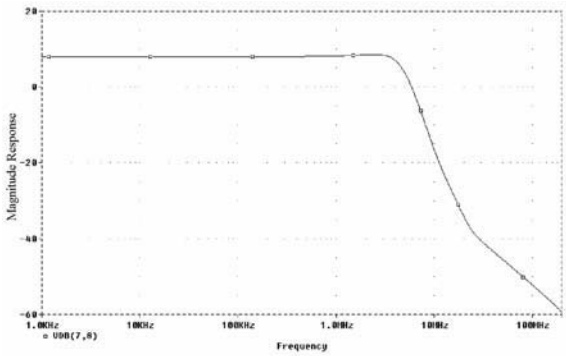

Fig. 13 The magnitude response of the fourth order fully differential filter.

VI. Conclusion

A CMOS FDCFOA has been introduced, analyzed and simulated. The FDCFOA is based on a novel class AB fully differential buffer circuit. The circuit is suitable for wide range, low voltage and low power applications. The proposed FDCFOA circuit is characterized by the ability to achieve high gain with low loss of bandwidth. Application examples in designing variable gain amplifier (VGA), fully differential integrator, and fourth order lowpass filter suitable for wideband CDMA systems are also provided.

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