Strategies for Quality and Performance Improvement of Hardware Verification and Synthesis Algorithms

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In this thesis, we are concerned with improving the quality and performance of different EDA algorithms particularly in area of hardware verification and synthesis. This thesis is organized as follows:

Chapter one presents thesis motivation, objectives, outlines, and research publications produced from our work.

Chapter two introduces the necessary background for the techniques used in this dissertation. It introduces the fundamentals of BDDs, including its concepts, algorithms. In addition, SAT-based Bounded Model Checking (BMC) is introduced. Static logic implications and their various types will also present. Preliminaries for timing-aware and low-power logic synthesis is introduced.

Chapter three introduces the detailed BDDs construction with Hopscotch hashing. We will introduce efficient resizing and garbage collector mechanism. We will presents The results for these algorithms.

Chapter four introduces the details of filtering algorithm of static implications. In addition, it will present the parallel framework for generating static implications. Finally, the results will be presented.

Chapter five introduces the details of our timing-aware synthesis algorithm. We apply TACUE in two different cutting strategies. In addition, we will present the parallel framework for generating the synthesized sub-cuts. Finally, the results will be presented.

Chapter six introduces the details of our Low-power synthesis algorithm. First, we introduce our problem and our proposed algorithm related concepts. Secondly, our scalable algorithm along with heuristics is introduced. Thirdly, Results and experiments are presented. Finally, our work is concluded.

Chapter seven presents the future work for this thesis. We propose to extend algorithms presented in Chapter three to very large BDDs and partition BDDs. In addition, we propose to filter Potential Inductive invariants to assist SAT solver to efficiently solve BMC problems. Finally, we propose to apply both BDDs and SAT techniques we have investigated to logic synthesis area.