Fayoum University

Faculty of Engineering

Electronics and Communications Engineering Department

Fault Diagnosis for Analog Circuits

A Thesis

Submitted in partial fulfillment of the requirements of the degree of

Master of Science in Electrical Engineering

(Electronics and Communications Engineering)

Submitted by

Mohamed Mostafa Mahmoud Ali Dakhil

B.Sc. of Communications and Electronics Engineering, Fayoum University 2016

Supervised by

Prof. Dr. Amr Mohamed Refaat

Faculty of Engineering, Fayoum University

Prof. Dr. Ahmed Hassan Madian

Faculty of Engineering, Nile University

Dr. Rania Fouad Ahmed

Faculty of Engineering, Fayoum University

ABSTRACT

In the present times, there is a trend of shrinking modern electronic devices which results in intricate circuits and systems. These systems typically consist of analog, digital or mixed-signal parts that are customized for specific applications via application-specific integrated circuits (ASIC) or system-on-chip (SoC). However, testing these advanced devices has become challenging with increasing costs. Thus it becomes necessary to streamline this process by seeking new robust techniques like automatic test plan generation (ATPG), one of the primary objectives in this field.

Analog circuits possess characteristics that can be described through various domains, such as DC, frequency, or time. In the instance of describing a circuit in the time domain it is reliant on a set of differential equations with order dependent upon how many separate energy-storage items are present within the circuit. Solving these equations requires numerical integration and has potential for computational complexity which may result in instability if high-order equations don't converge successfully. Conversely nonlinear designs have effective practicality too here.

In this thesis, we try to inspect the emerging trends for possible recent advances in analog systems design, and also for fault localization in analog circuits. Conventional and machine learning based algorithms are inspected and compared to hopefully reach an efficient, simple methodology for automatic design and testing of analog circuits.

We also inspect the technique to design and size the transistors of a symmetrical OTA to work in 65-nm process, with high gain, bandwidth, and low power consumption.

We also propose the usage of ANN-based model to detect and localize the faults in OTA circuit. The usage of such method proves to perfectly detect the single errors. With degraded performance for higher order errors.