Development of a Dual-core 64-bit MultiProcessor Based on the OpenSPARC Design

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Abstract

Multiprocessors were built as early as invent of computers. The topology & implementation techniques have developed over time. In the late 1990s multi-core processors implemented on single chip were designed and manufactured. Multiprocessors are implemented as multiple processing cores that are connected together by interconnect network. The memory may be a central shared memory or distributed amongst the processing cores. Multiprocessors were initially reserved for high end applications. Currently, Multiprocessors are on almost all personal computers.

SUN's OpenSPARC open core multiprocessor is an example of multiprocessors implemented on single chip. The multiprocessor system contains eight SPARC cores; each of which is a 64 bit four threaded processor conforming to the SPARC V9 ISA. Each core has its own local L1 cache memory. Additionally, there is a shared L2 cache memory for the eight cores. The L2 cache is divided into four banks and connected to the SPARC cores with interconnect network called CCX (CPU Cache Crossbar). Each L2 cache bank is connected to DDR2-SDRAM memory controller that is connected to external DDR2-SDRAM memory. Thus, the multiprocessor system has four memory channels.

The objective of this thesis is to implement a multiprocessor on an FPGA based on the OpenSPARC T1 powerful cores. We built on the OpenSPARC T1 design released by SUN. A multiprocessor system on Xilinx FPGA XC5VLX110T is implemented. The multiprocessor system consists of a) Two SPARC cores. b) Interconnect network c) Memory subsystem that represents the L2 cache banks and memory controller. Since the single SPARC core consumes large resources on the FPGA (approx. 95%), we started by simplifying the single core to reduce resource usage. After the core was simplified we implemented a dual-core system with the OpenSPARC CCX as interconnect network and Xilinx's embedded microprocessor Microblaze as memory subsystem which performs the function of the L2 cache banks,

memory controller, and cache directory controller. We implemented the system and evaluated its performance using the Dhrystone benchmark. The performance of the system was not satisfactory since the memory subsystem implemented using Microblaze processor created a performance bottleneck. So a second implementation was worked out in which we designed a custom memory subsystem implemented as pure hardware. The implemented memory subsystem is five stages pipelined and operates at a frequency higher than that of the SPARC core to avoid any bottlenecks. The new implementation improved the performance by more than 250% so the only limit on the performance is the SPARC core itself.