NOC SWITCH
TRAFFIC SIMULATION AND PERFORMANCE ENHANCEMENT

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ABSTRACT

Systems-on-Chip (SoC) is introduced to offer high performance to satisfy the increasing communication demands of complex VLSI circuits. SoC interconnects Intellectual Property cores (IPs) through busses. Large SoC leads to large power consumption and delay. Moreover, as the complexity of SoC increases, system scalability becomes a bottleneck. Network-on-Chip (NoC) is presented to solve the interconnection problem of large scale SoCs. In NoC, switches replace bus interconnections. NoC offer high scalability, reliability and high performance. Virtual Channel (VC) concept has been sponsored to enhance NoC performance and flow control. Virtual channels improve network throughput and link utilization at high load conditions.

VC reduces packet blocking by allowing multiple logical channels to share the same physical channel at switch port where non-blocked packets can bypass a blocked packet so that data transfers continue to be carried out. With employing an appropriate routing algorithm, VCs can eliminate packets deadlocks by minimizing the resource dependency. Moreover, quality of service is supported by virtual channels by associating priorities to logical channel sets so that a higher priority channel can bypass channels of lower priority. VCs provide guaranteed data transfer characteristics. Due to the extra cost of control and buffer implementation of virtual channels, VCs are tightly coupled with power, area, and latency of the NoC. As the number of idle virtual channels in NoC increases, large amount of leakage power is dissipated. The leakage power is expected to dominate the overall power consumption as the technology scales down.

Low leakage power switch allows saving in power dissipation of the NoC. Power supply gating is employed to reduce the leakage power dissipation. Two power reduction techniques are exploited to design low leakage power NoC switch. First, Adaptive Virtual Channel (*AVC*) technique is presented as an efficient technique to reduce the active area using hierarchical multiplexing tree of VC groups. Second, power gating reduces the average leakage power consumption of the switch via controlling the supply power of VC groups. The presented techniques save significant amount of the switch leakage power. In addition, the dynamic power is reduced.

Traffic-based Virtual channel Activation (*TVA*) algorithm is presented to determine traffic load status at the NoC switch ports. Consequently adaptation signals are sent to control the power gating unit to activate or deactivate virtual channel groups of the multiplexed VCs binary tree. *TVA* algorithm optimally utilizes virtual channels by deactivating idle VCs groups to guarantee high leakage power saving without affecting the NoC throughput. *TVA* activates virtual channels upon request.

TVA algorithm is an efficient and flexible algorithm that defines a set of parameters to be used to achieve minimum degradation in network throughput with maximum reduction in leakage power. Network average leakage power has been reduced for different topologies (such as 2D-Mesh and 2D-Torus) with negligible degradation in throughput. High level cycle accurate NoC simulator is developed in order to simulate the presented algorithm and techniques. Enhanced implementation of the presented techniques is explored for better leakage power savings. The implementation is simulated using the new simulator.