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ASYNCHRONOUS DESIGN FOR ROBUST NOC UNDER PROCESS VARIATION

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BY

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ABSTRACT

Synchronous Networks-on-Chip (NoCs) suffer from performance degradation mainly due to clock skew. Clock skew is more pronounced with process variation (PV). Asynchronous NoC have more immunity to PV than synchronous networks which would favor it in terms of network throughput. Architecture-Level simulator is developed to determine the ability of different NoC communication schemes to mitigate the impact of PV. The proposed simulator supports both synchronous and asynchronous NoCs. It is fully parameterized framework for modeling NoCs under PV with different technology nodes. The proposed simulator is validated against Circuit-Level simulator. For different technology nodes, delay components and throughput variation are determined for both synchronous and asynchronous networks.

Architecture-Level simulation shows that clock skew is the dominant delay component and the main cause of performance degradation in synchronous NoC. Clock skew represents 27% and 32% of synchronous NoC total delay variation for 45nm and 32nm technologies, respectively. Using real traffic, architecture-level analysis shows a considerable throughput reduction in case of synchronous NoC under PV conditions. Throughput degradation increases rapidly with advance in technology for synchronous NoC. 64-Cores synchronous NoC loses 30% of nominal throughput for 45nm technology and 41% of throughput for 32nm with PV. On the other hand, 64-Cores asynchronous network throughput degradation is only 12% and 13.6% for 45nm and 32nm, respectively. For different NoC sizes with different traffic workloads, throughput reduction for synchronous design is more than double the reduction of asynchronous design which unfavor the synchronous network from throughput points of view. Asynchronous scheme is preferable as technology scales.

A congestion aware, fault tolerant and PV aware adaptive routing algorithm (*CFPA*) is introduced for asynchronous NoCs. The proposed routing algorithm maintains two routing tables to determine the packet path: one for routing directions based on propagation delay (including PV delay) and the other to keep track of the queuing delays at each router port. The queuing delay is used as an indication for congestion. The proposed routing tables store

multiple paths to every destination via all polar directions, which makes *CFPA* a fault tolerant algorithm in case of path failures.

The proposed algorithm is verified against other popular routing algorithms for NoCs with different topologies and network dimensions. On average, *CFPA* enhances the NoC throughput by 60% compared to the recently proposed routing algorithms. With *CFPA*, the impact of faults on NoC throughput is alleviated by 48%. In addition, the average delay of messages routed using *CFPA* is shorter than that of other algorithms by (26~75) % under process variation conditions. Furthermore, the proposed algorithm minimizes the impact of PV on NoC throughput to less than 5% of the nominal throughput for mesh topology.