Heterogeneous MPSOC for Software Defined Radio of Long Term Evolution (LTE) 4G standard

Abstract

Mobile devices are becoming the dominant computing platforms in persons' life. Every day, more and more applications and tools are migrated to mobile devices including high bandwidth internet access, video conferencing and high definition multimedia. The standards and protocols used by all these applications are evolving rapidly in order to provide performance improvements and new features. Next generation mobile platforms need to take into consideration the rapid advances in standards and technologies.

Software Defined Radios (SDR) offer an efficient solution to keep up with technology advances by providing integration and utilization of existing and future wireless communications standards on a configurable hardware platform. To support the next generation wireless broadband standards, the SDR platforms must be powerful enough to support the increased bandwidth requirements.

One of the most processing intensive component in any SDR platform is the forward error correction decoder. Most of the available SDR platforms dedicate a co-processor for that task. Fourth generation wireless broadband standard uses Low-Density Parity Check codes (LDPC) for error correction because of their ability to provide high error correction performance for high bandwidth communication.

LDPC codes have become very attractive forward error correction technique for modern applications because of their Shannon limit approaching capability. The message passing algorithm is the name of a group of iterative algorithms that are used to decode LDPC codes. The exact algorithm name is based on the type of information that is exchanged or the type of operations that are performed, for example, bit-flipping, belief propagation, Sum-Product, and Minimum-Sum are all message passing algorithms.

Many hardware implementations for various message passing algorithms are available. Those implementations try to compromise between throughput performance, hardware complexity, and flexibility.

This thesis introduces an LDPC decoder that is capable of providing high bandwidth needed for next generation standards and at the same time, flexible to support future standards. It implements the message passing decoding algorithms with a combination of unicast and multicast communications between processing elements. The goal is to reduce the communication overhead and at the same time, keep the processing elements as simple as possible.

The suggested decoder works in one of two modes by implementing two decoding algorithms. The first mode implements the sum-product decoding algorithm that offers the best bit error rate (BER) performance making it suitable for modern communication applications requiring the most accurate error correction performance with moderate data rates.

The second mode implements the min-sum decoding algorithm which is much simpler and achieves even higher bitrates with acceptable BER performance degradation making it suitable for higher data rates applications with better SNR situations such as stationary WIFI hotspots and wired communications.

In order to implement the suggested LDPC decoder so that it becomes a part of an SDR system, flexibility to support different types of codes is a requirement that must be provided. That

flexibility is achieved by suggesting a new configurable, non-blocking interconnection network which is used to interconnect the processing elements of the decoder. That proposed network, we call it Selective-Benes and it is based on the famous Benes network.

The sum-product decoding algorithm used to decode LDPC is modified to increase its performance. The inherit algorithmic parallelism encourage a multiprocessing system implementation. Therefore, a multiprocessor architecture is suggested to support the modified decoding algorithm.

The two modes of operations of the decoder were simulated on MatLab to evaluate the bit error rate performance in each of them.

The decoder architecture was implemented on Virtex5 FPGA using VHDL in Xilinx ISE environment. Results show that the average resource requirements per processing element are much better than other implementations, making it feasible to implement the two decoding algorithms together. Working in the sum-product mode, the decoder can achieve up to 800 Mbps per iteration for a code length of 2640 with BER of 10^{-7} at 2.2dB. While working in min-sum mode, the decoder achieves up to 3.49 Gbps per iteration for a code length of 2640 with BER of 10^{-5} at 4.4dB.