Ali,M.K., Hamidian A., Malignaggi A., and Boeck G., "IQ Demodulator for the IEEE 802.15.3c Standard in the 90 nm CMOS Technology," European Microwave Conference (EuMC), 2014 44th, vol.6, no.9, pp.592-595, Oct. 2014.

Abstract: The design of an IQ-Demodulator for the IEEE 802.15.3c standard is presented. The design is targeted for low noise, low power consumption and small chip area. The IQ-Demodulator is fabricated in a 90 nm CMOS technology; it converts down a 2 GHz wide channel at around the IF of 20 GHz to the neighborhood of the zero frequency. New current bleeding network with resonating inductors is used for the direct-conversion mixer to mitigate the flicker noise effect, while other techniques are used to lower the DC current of the frequency divider at the required operating frequency. The conversion gain of the IQ-Demodulator is 6 dB and its input referred compression point -12 dBm. The demodulator consumes a total power of 50 mW. The total chip size including pads is 0.84×1.15 mm^2.