Ali M.K., V. Subramanian, T. Zhang, and G. Boeck, "Design of Ka-Band Miller Divider in 130 nm CMOS," in Radio-Frequency Integration Technology (RFIT), 2011 IEEE International Symposium on, pp. 205–208, Nov. 2011.

Abstract: This work presents the design techniques involved in the realization of CMOS Miller dividers operating in Ka-band frequencies. It will be shown that through a clear understanding of the conditions for stable divider operation, it is easy to design and achieve the optimum performance in terms of required input power, bandwidth for correct division, and power consumption. On-chip inductors are designed as to produce sufficient Q-factor enough to guarantee high loop gain yet wide bandwidth. The designed divide-by-two Miller divider is realized in a 130-nm CMOS technology with a chip area of 680×640 μm^2. The realized circuit achieves its optimum at 28 GHz with 10 GHz signal bandwidth. An output power higher than -16 dBm and a minimum required input power values lower than -2 dBm over the whole bandwidth have been measured. The divider consumes 10 mW including the 2 mW for the output balun from a 1.2 V power supply.