New 1.5-V CMOS second generation current conveyor based on wide range transconductor

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Abstract   This paper presents a novel CMOS low-voltage
and low-power positive second-generation current conveyor
(CCII +). The proposed CCII + uses two n-channel differ-
ential pairs instead of the complementary differential pairs;
i.e. (n-channel and p-channel), to realize the input stage. This
solution allows almost a rail-to-rail input and output opera-
tion; also it reduces the number of current mirrors needed in
the input stage. The CCII + is operating at supply voltages of
± 0.75 V with a total standby current of 133 μA. The applica-
tion of the proposed CCII + to realize a MOS-C second or-
der maximally flat low-pass filter is given. PSpice simulation
results for the proposed CCII + and its application are given.

Keywords   CMOS · Current conveyor · Low-power ·
Low-voltage · Rail-to-rail

1 Introduction

The second-generation current conveyor (CCII) proposed by
Sedra and Smith in [1] has proved to be a functionally flexi-
ble and versatile block. CCII circuits have been widely used
in high frequency analog signal applications like filters [2–5]
and current-mode oscillators [6, 7]. CCII based filters uses
the passive elements to realize the filter coefficients, while
transconductor capacitor filters ($G_m - C$) utilize the transcon-
ductance G_m of a transconductor to realize its time constant.

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One disadvantage of $G_m - C$ filters is their need for some
sort of tuning circuitry. Tuning is required because the filter
coefficients are determined by the product of two dissimilar
elements, such as capacitance and transconductance.

The CCII is a three terminal device derived by intercon-
necting the voltage and current followers. The Y terminal
is a high impedance terminal while the X terminal is a low
impedance one. The input voltage V_Y applied across the Y
terminal is conveyed to the voltage V_X across the X terminal;
i.e. ($V_X = V_Y$).

The input current applied to the X terminal is conveyed
to the Z terminal; i.e., ($I_Z = I_X$). The Z terminal is high
impedance output node suitable for current output. The di-
rection of the Z terminal current relative to the X terminal
current defines whether the CCII is positive (CCII +); i.e.,
($I_Z = I_X$) or negative (CCII–); i.e., ($I_Z = -I_X$).

The input-output relation could be described by the fol-
lowing matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \qquad (1)$$

Several CCII structures have been realized [8–28], these
structures aimed at improving the voltage and the current
transfer accuracy [8], increasing the output current capabili-
ties [15, 16], while reducing the offset using several compen-
sation techniques [17], and to realize a differential voltage
current conveyor (DVCC) [19, 20]. In addition, a fully differ-
ential behavior realization has been presented [21–24]. To ex-
tend the region of operation up to rail-to-rail, the input stage
is made of two parallel connected complementary differen-
tial pairs; i.e., (n-channel and p-channel) [25]. Unfortunately,
it includes a class A output stage which limits the maximum
output current achievable. However, with this approach, an

increase in the supply requirements to a value higher than 3 V is needed. In [26], a low-voltage, a low-power, and a rail-to-rail input/output ranges CCII + capable of operating under a minimum supply voltage of $(V_T + 3V_{DSsat})$, as well as, high driving current capability, using the same two parallel connected complementary differential pair input stage is given. However, with this approach the small and large signal behaviors still suffer from large transconductance deviation when the high impedance input voltage sweeps the entire voltage range. Also, it requires using three matched pairs of current mirrors in the input stage to sum the currents of the complementary differential pairs and this affects the bandwidth and the offset voltage between the X and Y terminals.

In this paper, a new low-voltage CMOS CCII + capable of operating under a minimum supply voltage of $(2V_{DSsat} + V_{SDsat})$ for the input stage and $(|V_{Tp}| + V_{Tn} + V_{DSsat})$ for the output stage is proposed. The new CCII + is based on using two parallel connected n-channel differential pairs instead of the traditional two parallel connected complementary differential pair to realize the input stage. This reduces the number of current mirrors required to obtain input stage to only one current mirror which help to improve the input stage bandwidth and reduces the offset voltage. The class AB current follower stage used to provide rail-to-rail high-current driving capability operation.

This paper is organized as follows, In Section 2, the circuit description and CMOS realization of the proposed CCII + is illustrated, the channel-length modulation and the mismatching effects have been discussed. In Section 3, PSpice simulations of the proposed CCII + using CMOS 0.35 μm technology and simulation comparison between the proposed CCII + and the one presented in [26] are also given. In Section 4, an application example of realizing a MOS-C second-order maximally flat low-pass filter using proposed CCII + is given. In Section 5, conclusion has been drawn.

2 The proposed CCII + CMOS realization

The block diagram [27, 28] of the proposed CCII + is shown in Fig. 1. The scheme includes three transconductors: G_1 is a proposed differential input wide range transconductor amplifiers, G_2 and G_3 are two matched transconductance output stages, their inputs are connected together. The voltage follower stage of the CCII + consists of G_1 and G_2 closed loop negative feedback structure. To convey the current from the X terminal to Z terminal a replicate from the output stage (G_3) is used. In the following subsections, the CMOS realization of the three main blocks, shown in Fig. 1, will be illustrated.
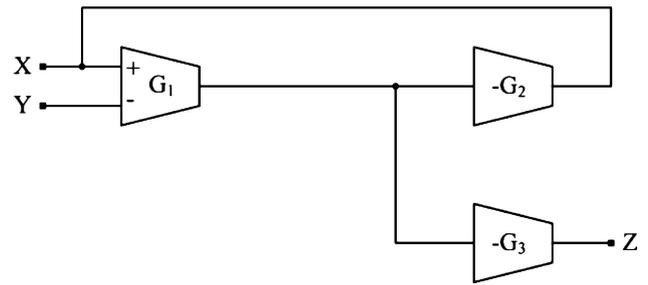
Fig. 1 The G block diagram of the CCII + [27, 28]

2.1 Circuit description

The CCII + structure begins with the differential input wide range transconductor amplifier (G_1). The CMOS realization of the wide range transconductor, shown in Fig. 2, consists of two matched parallel connected n-differential pairs (M_1, M_2) and (M_3, M_4), two matched biasing current source transistors (M_5, M_6) (G_1), cascode current mirror formed of two matched transistors (M_7, M_8) and transistor (M_9), two pairs of matched source followers transistors (M_{10}, M_{11}) and (M_{12}, M_{13}). Transistors M_5 and M_6 carry equal bias currents (I_B) while transistors (M_{10}, M_{11}) and (M_{12}, M_{13}) produce a positive voltage shift for the input voltage applied on transistor M_{11} and M_{13}, respectively. All transistors are operating in the saturation region; the control voltage V_C applied to transistors M_{10} and M_{12} gates controls the shifting value as follows,
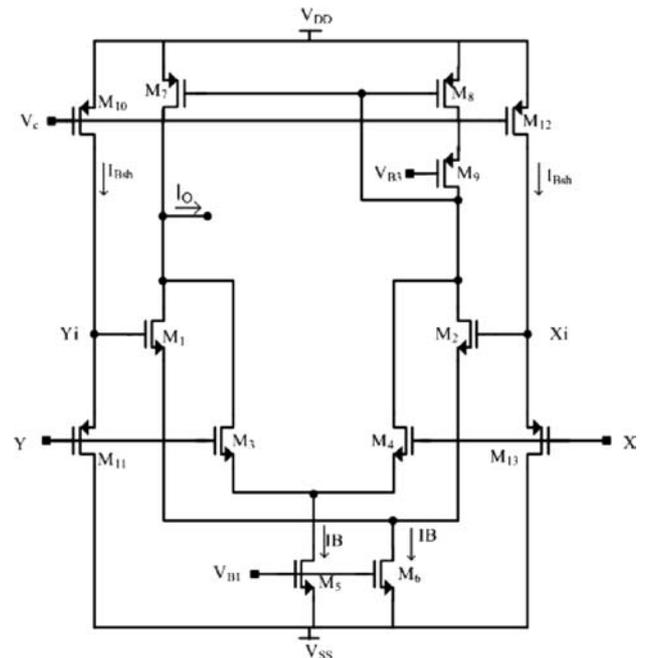
Fig. 2 The CMOS realization of the wide-band transconductor circuit

$$V_{Yi} = V_Y + (V_{DD} - V_C) \tag{2}$$

$$V_{Xi} = V_X + (V_{DD} - V_C) \tag{3}$$

where V_{Yi} and V_{Xi} are the output voltage from the source followers, V_Y is the high input impedance voltage, and V_X is the low input impedance terminal.

The circuit regions of operation could be explained as follows, for V_Y, V_X voltage close to the negative supply voltage V_{SS} ($V_{SS} \leq V_Y, V_X < 2V_{Tn} + V_{SS}$), So the current source transistor M_5 and, hence, the differential pair M_3 and M_4 are cut-off. Then, the small and large signal behaviour of the whole circuit result only from the contribution of the differential pair M_1 and M_2, biased with current source transistor M_6. In the middle range ($2V_{Tn} + V_{SS} \leq V_Y, V_X < V_C + 2V_{Tn} - 2V_{DD}$), both input pairs ($M_1$–$M_2$) and ($M_3$–$M_4$) are active and the small and large signal behaviour of the whole circuit result from the contribution of both differential pairs. Finally when V_Y, V_X very close to V_{DD} the positive supply voltage ($V_C + 2V_{Tn} - 2V_{DD} \leq V_Y, V_X \leq V_{DD}$), the current sources of the shifters M_{10} and M_{12} are cut-off. Therefore, the small- and large signal behaviour of the whole circuit contribution result only from the differential pair M_3 and M_4 biased with current source transistor M_5. This ensures a rail-to rail operation. Assume that, the input differential pairs are matched and all transistors are operating in the saturation region. The output current could be obtained as follows,

$$I_o = \begin{cases} \frac{K_n}{2}(V_Y - V_X)\sqrt{\frac{4I_B}{K_n} - (V_Y - V_X)^2} & (V_{SS} \leq V_Y, V_X < 2V_{Tn} + V_{SS}) \\ K_n(V_Y - V_X)\sqrt{\frac{4I_B}{K_n} - (V_Y - V_X)^2} & (2V_{Tn} + (V_{SS} \leq V_Y, V_X < V_c + 2V_{Tn} - 2V_{DD}) \quad . \\ \frac{K_n}{2}(V_Y - V_X)\sqrt{\frac{4I_B}{K_n} - (V_Y - V_X)^2} & (V_C + 2V_{Tn} - 2V_{DD} \leq V_Y, V_X \leq V_{DD}) \end{cases} \tag{4}$$

where K_n is the transconductance parameter of the matched differential pairs, and I_B is the biasing current of the differential pairs.

It is apparent from Eq. (4) that this structure does not provide constant transconductance over the variations of the input voltages V_Y, V_X. A feed forward section could be added to guarantee a constant transconductance over the variations of the input voltages V_Y, V_X. However this is not a real drawback so long as the loop gain is sufficiently high. Indeed, variations of the open loop parameter were greatly reduced by feedback action.

The structure of the CCII + input stage (voltage follower) requires that the X terminal must have low input impedance. So, a suitable buffer circuit should be used to fulfill this condition and to provide a rail-to-rail swing capability. Figure 3 gives the CMOS realization of the CCII + input stage; transistors (M_{14}–M_{20}) fulfill the required buffering action with a rail-to-rail swing capability. Transistors M_{14} and M_{15} (G_2)

forms the push pull output stage at the X terminal, transistors M_{16} and M_{17} are level shifting transistors providing proper biasing for transistor M_{15}. This push pull action of M_{14} and M_{15} reduce the power dissipation. To prevent the cross over distortion, both transistors M_{14} and M_{15} must be ON when no current is withdrawn from the X terminal (standby mode), this current should be small and controllable. This is achieved by using a suitable gate voltage of M_{20}, which sets the voltage level shift between the gates of M_{14} and M_{15}. The standby power consumption of the overall circuit for dual power supply is given by:

$$P_{SB} = 2V_{DD}(3I_{SB} + 2I_B + 2I_{Bsh} + I_{B1}) \tag{5}$$

The last term in the above equation is the current passing through the level shift transistors (M_{16}, M_{17}). This current can be kept small by choosing small aspect ratio for transistors (M_{16}, M_{17}). The class AB output stage enables the circuit to derive the heavy resistive and capacitive load with low standby power dissipation and no slewing. It is worth mentioning that smaller miller compensation capacitors can be connected between the gate and drain of transistors M_{14} and M_{21} to ensure good transient response under all loads.

Transistors M_7 and M_8 forces the current in transistors M_1 and M_3 to be equal to the current in transistors M_2 and M_4. Therefore,

$$I_{M1} + I_{M3} = I_{M2} + I_{M4} \tag{6}$$

From the above equation, the matched differential pair transistors carry equal currents. Therefore,

$$V_X = V_Y \tag{7}$$

Finally, the CMOS realization of the CCII + is completed by adding a current follower stage, as shown in Fig. 4, which is made up of transistors (M_{21}, M_{22}) (G_3). The X terminal current is conveyed to the Z terminal current through the current follower stage. Therefore,

$$I_Z = I_X \tag{8}$$

The CMOS realization of the CCII + block diagram shown in Fig. 1 is given in Fig. 4, where, transistors (M_1 to M_6), (M_{14}, M_{15}), and (M_{21}, M_{22}) realize blocks G_1, G_2, and G_3 respectively.

Fig. 3 The CMOS realization of the CCII + input stage voltage follower circuit
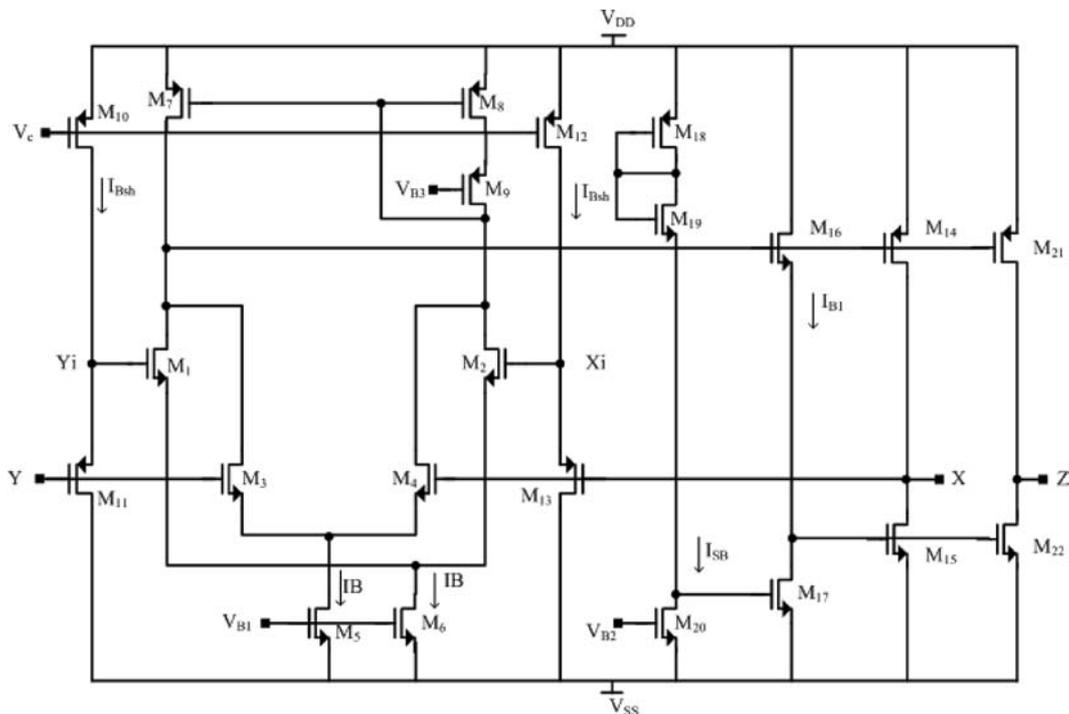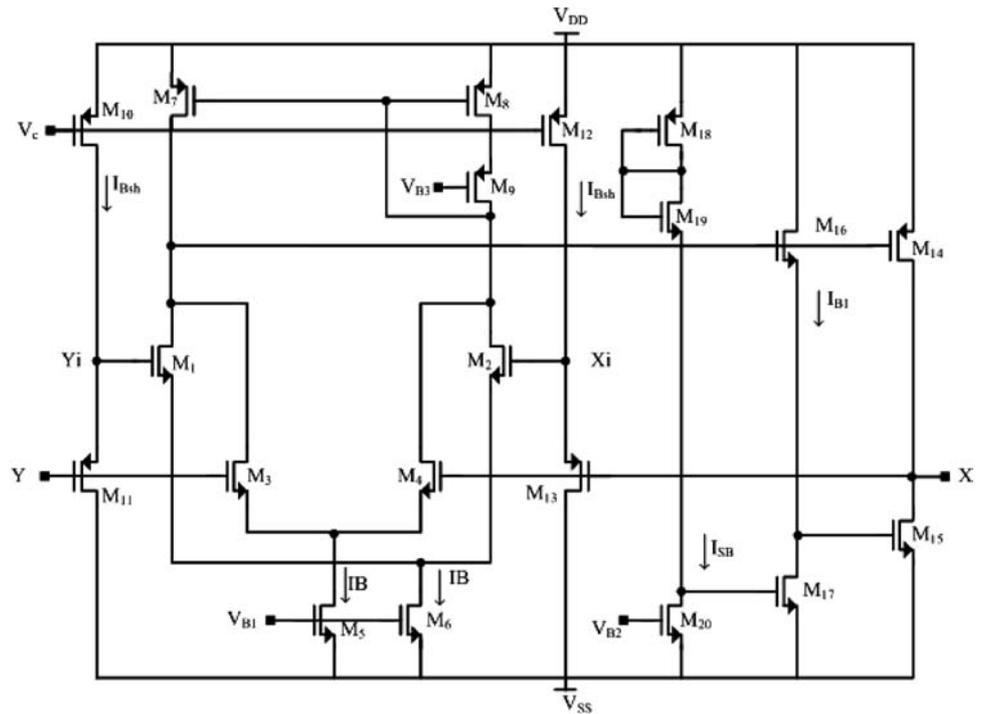
Fig. 4 The complete CMOS realization of the proposed CCII + circuit

It is worth to mention that, the proposed CCII + input stage is a dual circuit. This means that when the input stage formed from transistors M_1 to M_6 changed to PMOS, the current source formed from transistors M_7 to M_9 and the biasing circuits M_{10} to M_{12} will be NMOS and vice versa.

2.2 Circuit small-signal analysis

The loop gain by blocks G_1 and G_2 mainly determines the accuracy of the voltage transfer gain and the resistance at X terminal. When both differential stages

are properly working the open-loop gain T is given by,

$$T(s) = T_{G_1}(s) \cdot T_{G_2}(s) \tag{9}$$

Where $T_{G_1}(s)$ and $T_{G_2}(s)$ are the voltage gains related to blocks G_1 and G_2, respectively, and their DC expressions could be represented as follows,

$$T_{G_1}(0) = G_1 \cdot r_{O1} = \left(\left(\frac{g_{m11} \cdot (r_{ds11}//r_{ds10})}{1 + g_{m11} \cdot (r_{ds11}//r_{ds10})} \right) \right.$$
$$\left. \cdot g_{m1(or2)} + g_{m3(or4)} \right) \cdot (r_{ds7}//r_{ds1}//r_{ds3}) \tag{10}$$

$$T_{G_2}(0) = G_2 \cdot r_{O2} = g_{m14} \cdot (r_{ds14}//r_{ds15}) \tag{11}$$

In the above equations r_{o1} and r_{o2} are the output resistances of blocks G_1 and G_2 as shown in Fig. 1, g_{mi} and r_{dsi} are the transconductance and the drain to source resistance of the ith transistor where i is the transistor number. As a result for the feedback, as shown in Fig. 1, the voltage gain between the terminals Y and X becomes,

$$Av(s) = \frac{1}{1 + \frac{1}{T(s)}} \tag{12}$$

Which tends to 1 for high values of $T(s)$ the input resistance at the X terminal is approximately given by,

$$r_X \approx \frac{r_{o2}}{T(0)} = \frac{(r_{ds14}//r_{ds15})}{T(0)} \tag{13}$$

The output resistance at terminal Z is simply obtained as follows,

$$r_Z = r_{o3} = r_{ds21}//r_{ds22} \tag{14}$$

where r_{o3} is the output resistance of G_3 block shown in Fig. 1. If higher output resistances are needed, cascoded topologies can be used to increase this value as well as to improve the linearity performance.

2.3 Channel length modulation effect

The analysis in the pervious section neglects the channel-length modulation effect, which causes an offset voltage between the Y and X terminals. This offset voltage, which is mainly due to the channel-length modulation effect, can be compensated by appropriate choice of the transistors aspect ratios. The drain current of the PMOS transistor in the saturation region taking into account the channel length modulation is:
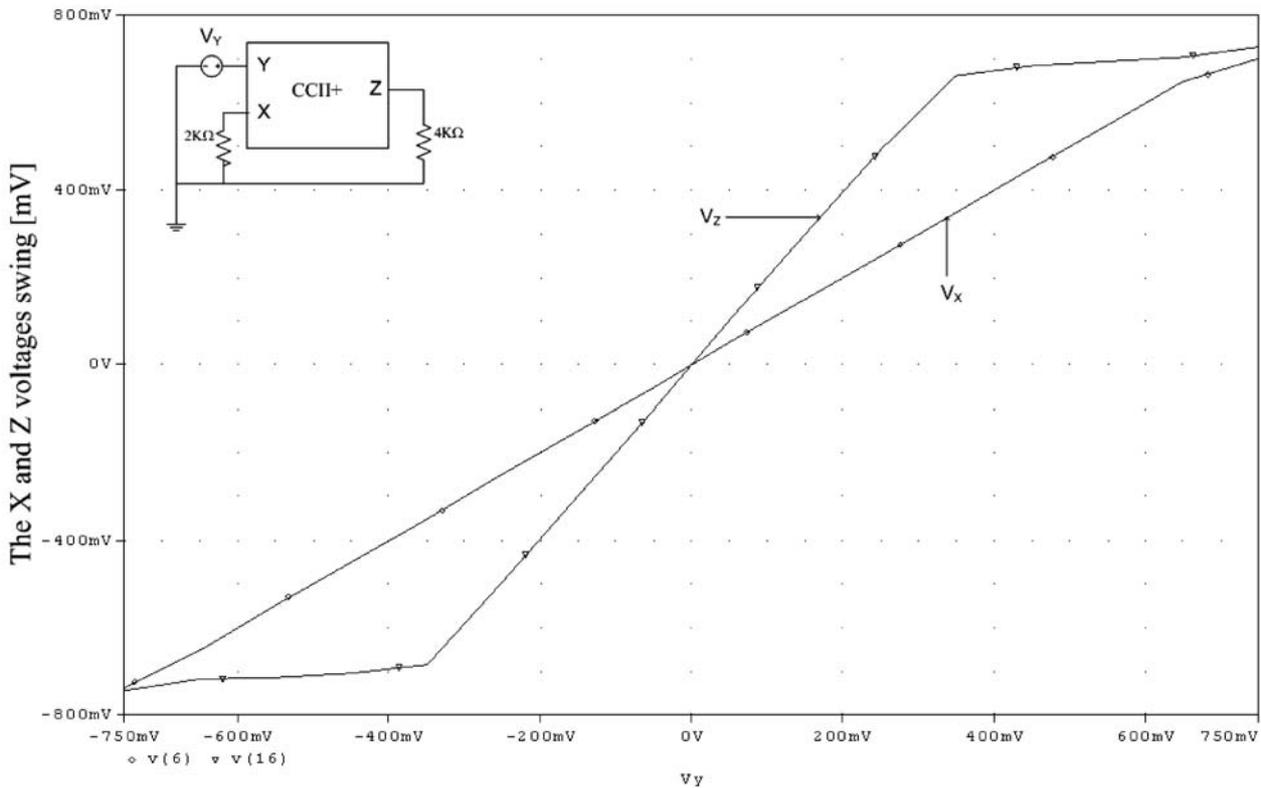
Fig. 5 The voltage swings V_Z and V_X of the CCII+ based amplifier with gain two

$$I_D = \frac{K}{2}(V_{SG} - |V_{TP}|)^2(1 + \lambda V_{SD}) \tag{15}$$

where $K = \mu C_{ox} \frac{W}{L}$ and λ is the channel length modulation parameter. Although the current mirror formed with transistors M_7 and M_8 have the same gate and source voltages, still there will be a current transfer error since the drain voltages are different. The current in M_7 will be given by:

$$I_7 = I_8 [1 + \lambda (V_{D8} - V_{D7})] \tag{16}$$

This dependence of the current on the drain voltage causes an offset voltage to appear at the X terminal. From Eq. (16) it may be concluded that the current transfer error in transistors M_7 and M_8 is proportional to the current they are supposed to carry. A cascode current mirror is used to compensate the current transfer error between the current mirror transistors. Transistor M_9 maintains the drain voltage of transistor M_8 nearly constant and independent on the voltage of the drain transistors M_2 and M_4. Transistor M_9 has large aspect ratios to ensure that the variations in the drain voltages of the transistor M_8 are small even for large current values. Also the channel length modulation effect can be reduced using longer channel length transistors to reduce λ.

2.4 Mismatching effect

Equations (4) and (5) was based on the assumption that the transistors forming two n-channel differential pairs (M_1–M_2) and (M_3–M_4) and the transistors forming current mirror (M_7–M_8) are matched. In this section, the mismatching effect will be discussed.

Referring to the circuit shown in Fig. 4, assume that M_7 has transconductance parameter equals K_7, and M_8 has transconductance parameter equals $K_7 + \Delta K_7$. Then, Eq. (4) could be written as follows,

$$\frac{K_7}{2}(V_{sG7} - |V_{Tp}|)^2 = \frac{K_7 + \Delta K_7}{2}(V_{sG8} - |V_{Tp}|)^2 \tag{17}$$

$$I_7 = I_8 + \Delta I_8 \tag{18}$$

Transistors M_7 and M_8 has the same source to gate voltages. Therefore, the percentage error due to mismatching effect is constant and could be obtained as follows,

$$\%error = \frac{\Delta I_8}{I_7}\% = \frac{\Delta K_7}{K_7}\% \tag{19}$$

This error appears as an offset voltage between the X and Y terminals and it can be enhanced by adopting a careful layout style.

3 Simulation results

The performance of the proposed CCII+ circuit was verified by performing PSpice simulations with supply voltages ± 0.75 V using 0.35 μm CMOS technology parameters and transistors aspect ratios given in Table 1. Figure 5 shows the output voltages X and Z when CCII+ used to realize amplifier with gain equals two. The Y terminal voltage is scanned from -0.75 V to 0.75 V while the X and Z terminals are terminated with 2 kΩ and 4 kΩ respectively. The total standby power dissipation is 0.213 mW. Figure 6 shows the variations of the offset voltage across the X terminal versus the variation in the input current applied across X terminal (I_X) when V_Y is equal to zero. The X terminal input resistance R_X is less than 7 Ω and the offset voltage is less than 2.5 mV at $I_X = 500$ μA. Figure 7 shows the Z terminal output current versus changes of the X terminal input current, where, I_X is changed from -1 mA to 1 mA. Figure 8 shows the current-drive capability of the proposed CCII+, a ± 0.75 V input sweep voltage was applied at the Y terminal, the output voltage obtained at the Z terminal, which is loaded with a 500 Ω output resistance. Figure 9 shows the open circuit voltage response between the Y and X terminals, where, V_Y is the AC-Varying signal with 1 V magnitude. The CCII+ has an open circuit 3-dB bandwidth of 10.5 MHz and the voltage transfer error of -0.012 dB. Figure 10 shows the short circuit current response between the X and Z terminals, where, I_X is the AC-varying signal with 100 μA magnitude. The CCII+ has an short circuit 3-dB bandwidth of 6.2 MHz, the current transfer error of -0.037 dB and the phase margin of $68°$. The input and output referred noise spectral densities are given in Fig. 11, the input and output noise are less than 700 nV/$\sqrt{\text{Hz}}$. The power supply rejection-ratio (PSRR) from the positive supply to the output is 80 dB and from the negative supply to the output is 84 dB. Table 2 gives the simulated results of the proposed CCII+ and compares it with the simulated result of the CCII+ circuit presented in [26]; both circuits have been simulated using PSpice.

Table 1 Transistors aspect ratios of the proposed CCII+

Transistors	W (μm)	L (μm)
M_1–M_4,	2.1	1.4
M_5, M_6	2.1	0.7
M_7, M_8, M_9	98	2.1
M_{10}, M_{11}, M_{12}, M_{13}	1.4	0.7
M_{14}, M_{18}, M_{21}	250.25	0.7
M_{15}, M_{22}	94.85	0.7
M_{16}, M_{17}, M_{19}, M_{20}	1.4	0.7
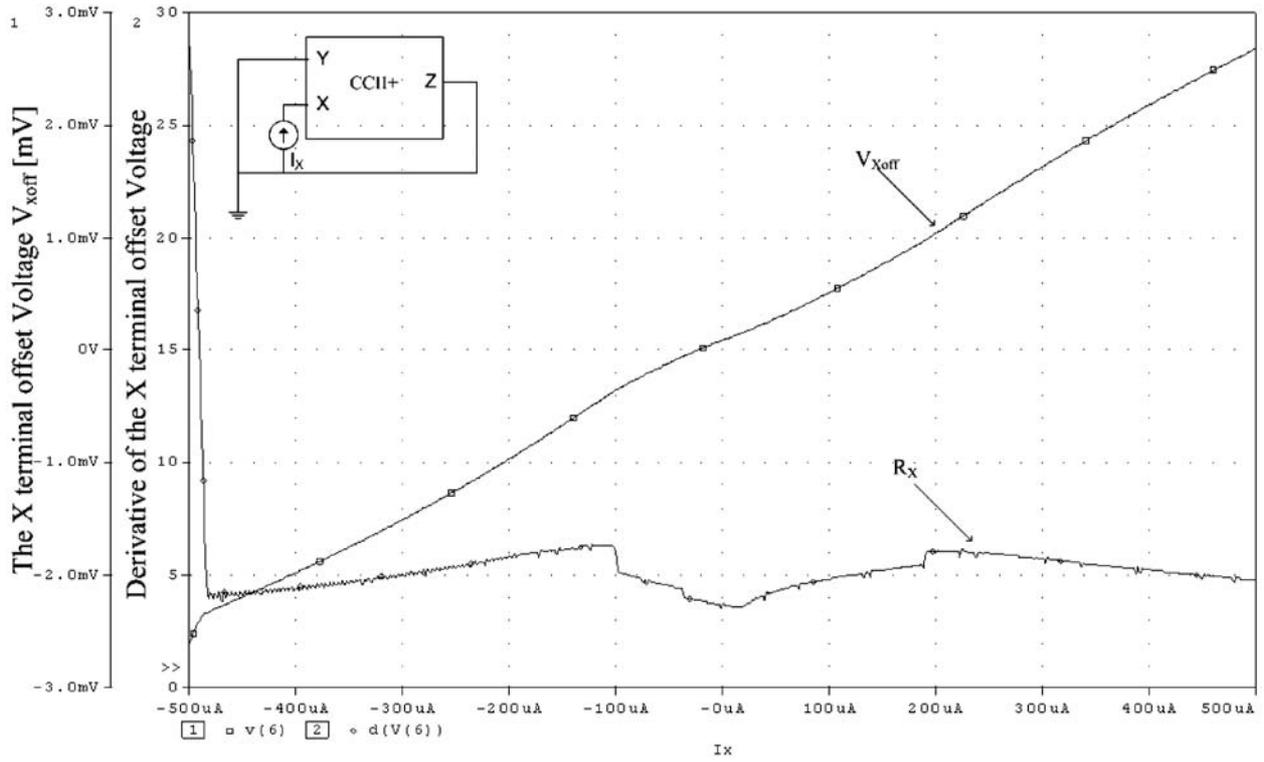
Fig. 6 The offset voltage of the X terminal along with its derivative
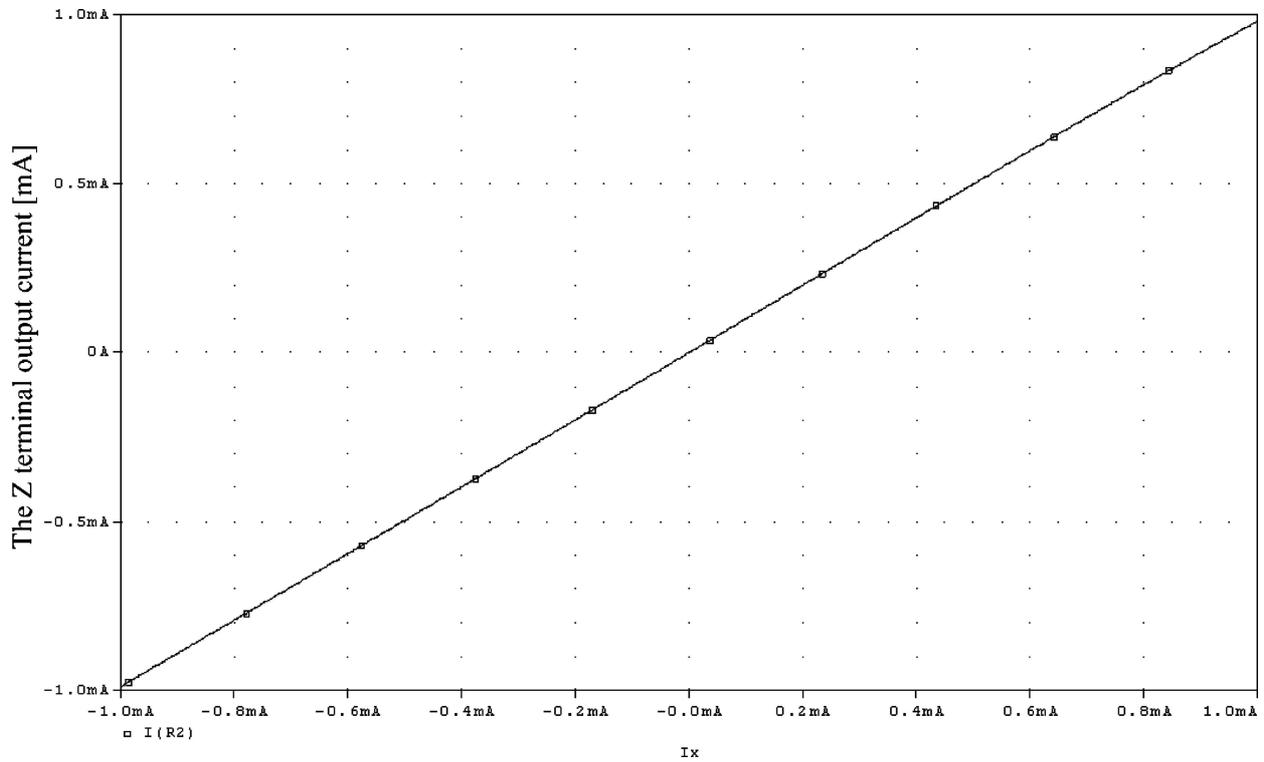
Fig. 7 The Z terminal output current versus changes of I_X
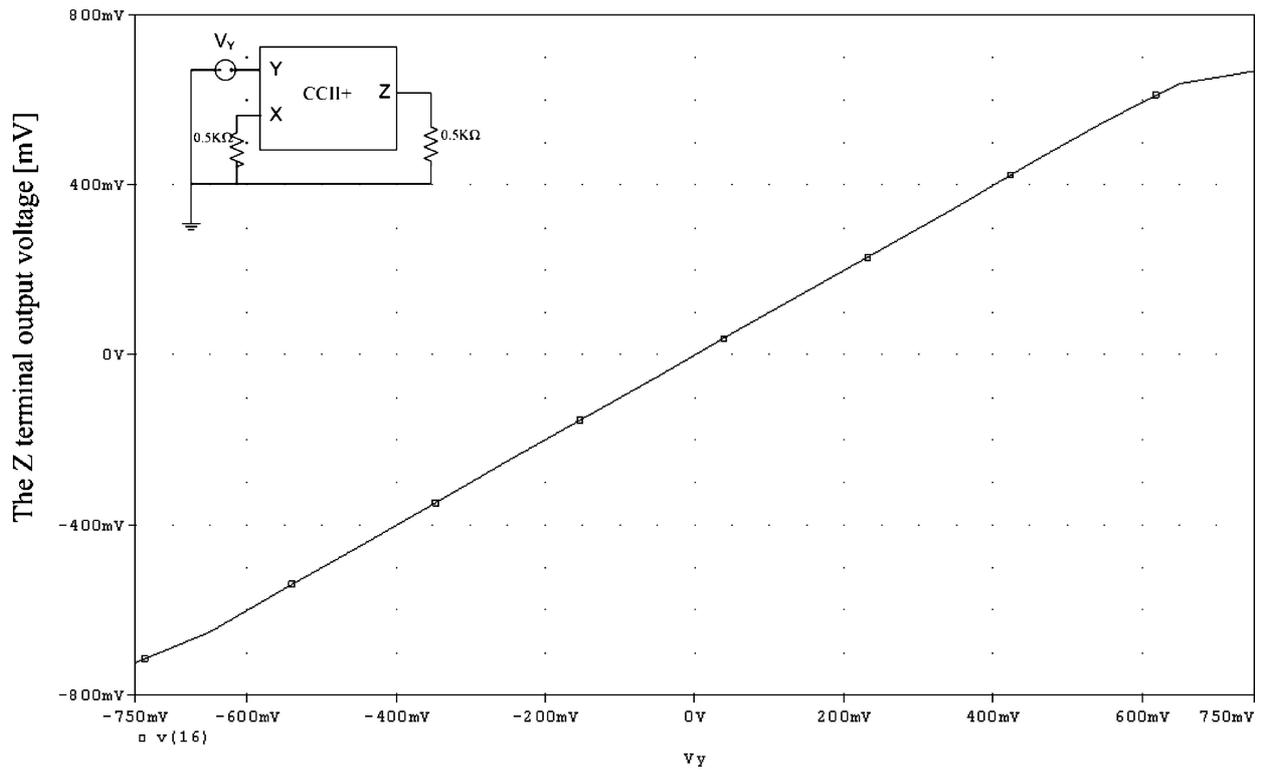
Fig. 8 The Z terminal output voltage versus changes of V_Y
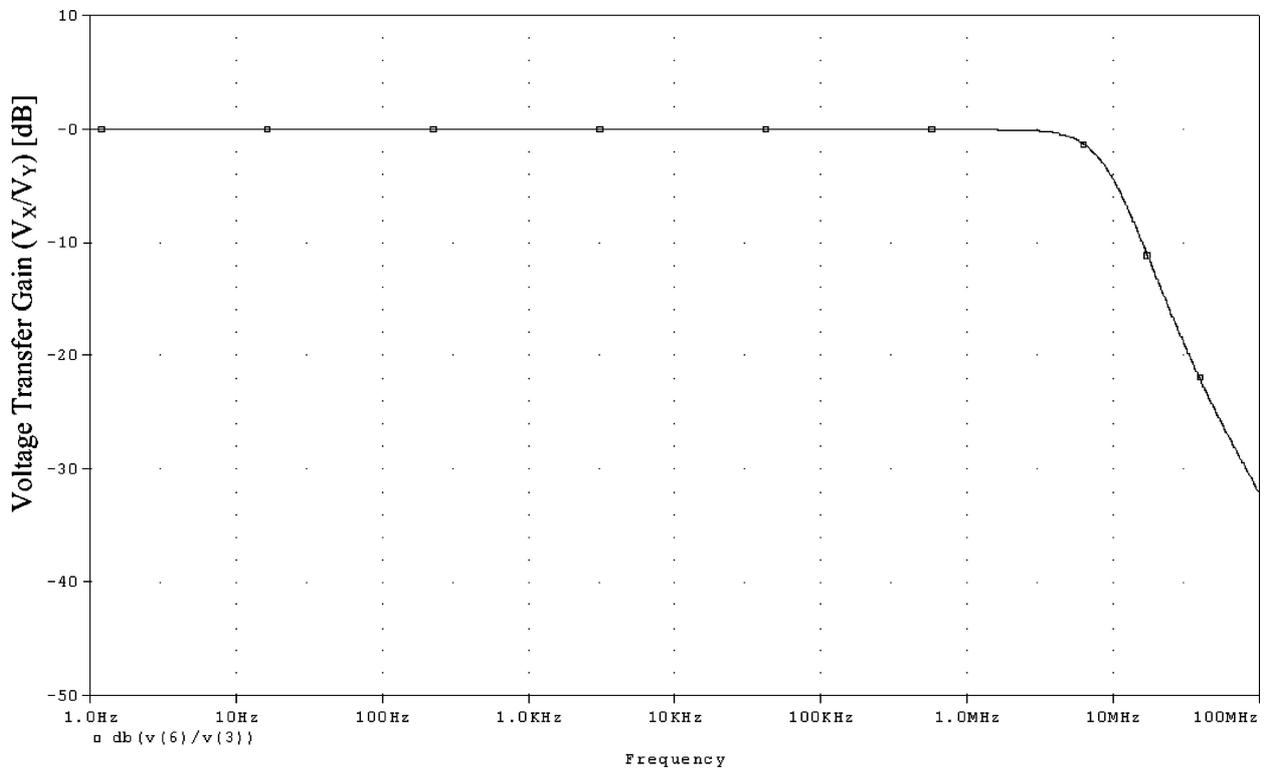
Fig. 9 Frequency response of the voltage transfer gain
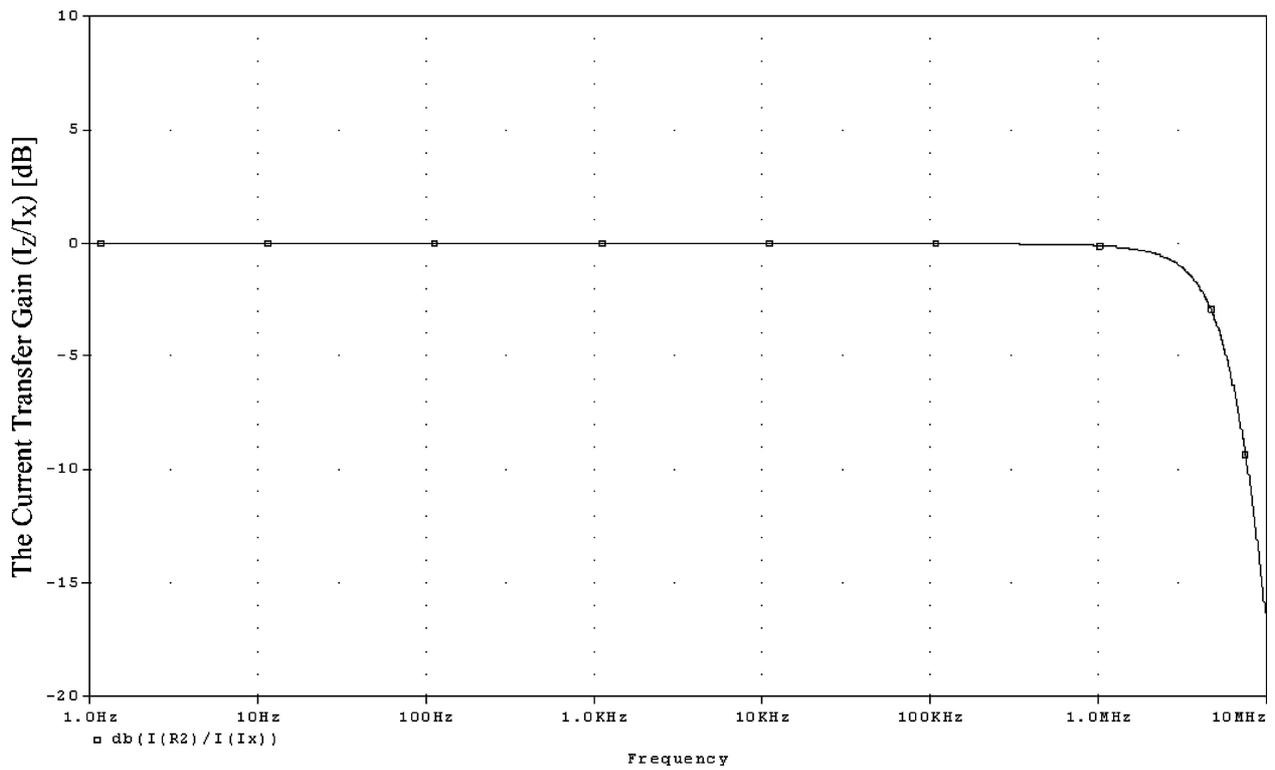
Fig. 10 Frequency response of the current transfer gain
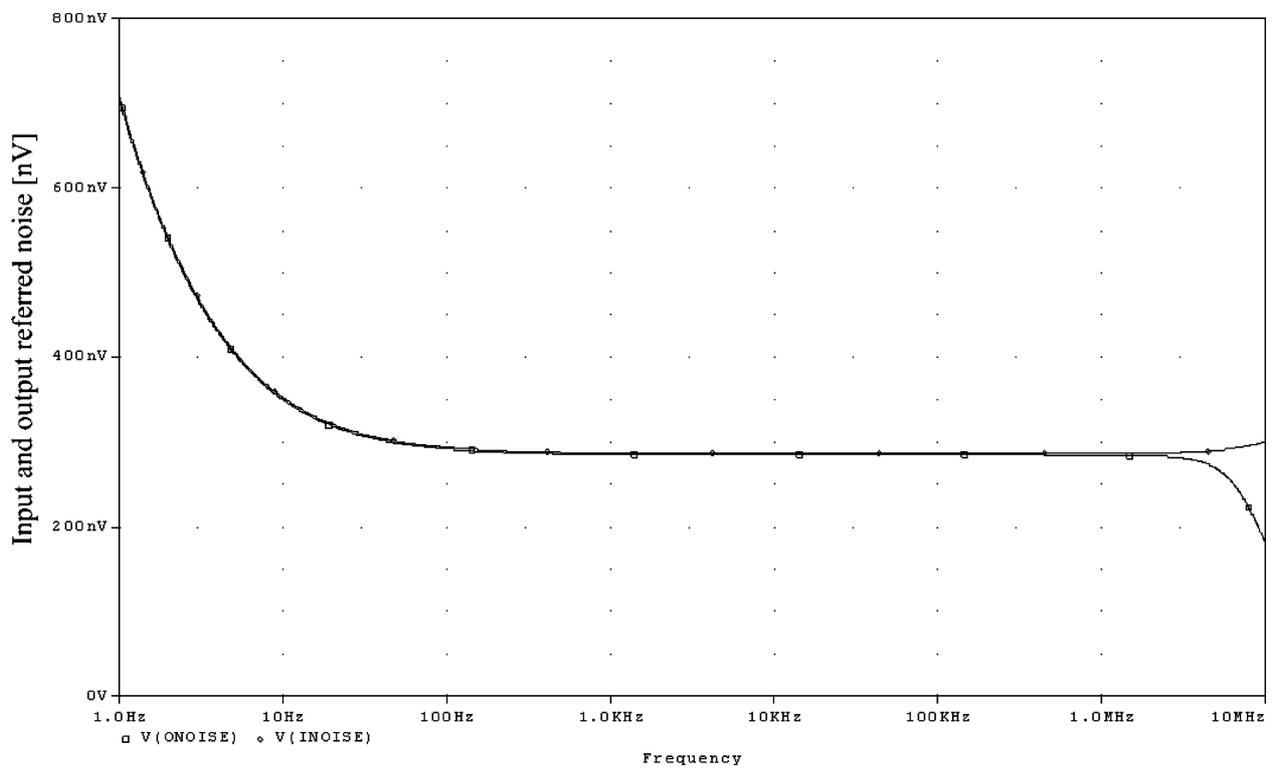
Fig. 11 The input and output referred noise spectral densities of the proposed CCII +

Table 2 Simulation results of the proposed CCII + as compared with the CCII + simulation results of [26]

Parameters	Proposed CCII +	CCII + in [26]
CMOS Technology	$0.35\ \mu$m	$0.35\ \mu$m
Power supply (V_{DD}, V_{SS})	(0.75 V, -0.75 V)	(0.75 V, -0.75 V)
No. of transistors	22	24
The 0.1% settling time	$<2\mu$ s	$<2\mu$ s
Total Power dissipation	0.213 mW	0.26 mW
The open circuit X terminal THD @ $V_Y = 0.5 * \sin(2\Pi f)$ V	-53 dB @ 1 KHz	-50 dB @ 1 KHz
Input Voltage Dynamic range ($I_x = 0$A)	-0.65 V to 0.65 V	-0.5 V to 0.5 V
The X terminal offset voltage while Y and Z are grounded	<2.5 mV	<3.5 mV
Current driving capability	-1 mA, $+1$ mA	-1.2 mA, $+0.9$ mA
Voltage transfer error	-0.012 dB	-0.02 dB
R_X	$< 7\ \Omega$	$< 15\ \Omega$
Current transfer error	-0.037 dB	-0.04 dB
The X terminal open circuit B.W	10.5 MHz	5.4 MHz
The Z terminal short circuit B.W	6.2 MHz	3 MHz

4 Application

The proposed CCII + has been used to realize a MOS-C second-order maximally flat low-pass filter as shown in Fig. 12. The proposed circuit employs four CCII + blocks, transistors (M_{1a}, M_{2a}), (M_{1b}, M_{2b}), and (M_{1c} to M_{4c}), and two grounded capacitor C_1, C_2. All transistors are operating in the linear region. By direct analysis, the following transfer function could be obtained:

$$\frac{V_{LP}}{V_{in}} = \frac{\frac{G_a G_c}{C_1 C_2}}{s^2 + s\frac{(G_b - G_a)}{C_1} + \frac{G_b G_c}{C_1 C_2}} \qquad (20)$$

Therefore,

$$\omega_O = \sqrt{\frac{G_b G_c}{C_1 C_2}} \quad \text{and} \quad Q = \sqrt{\frac{C_1}{C_2} \frac{G_b G_c}{(G_b - G_a)^2}} \qquad (21)$$

Where,

$$G_a = K_a V_{G12a}, \, G_b = K_b V_{G12b}, \, \text{and} \, G_c = K_c V_{G12c} \qquad (22)$$

From Eq. (21), the transconductance G_a controls the Q of the filter without affecting ω_O of the filter, to simplify the design, take:
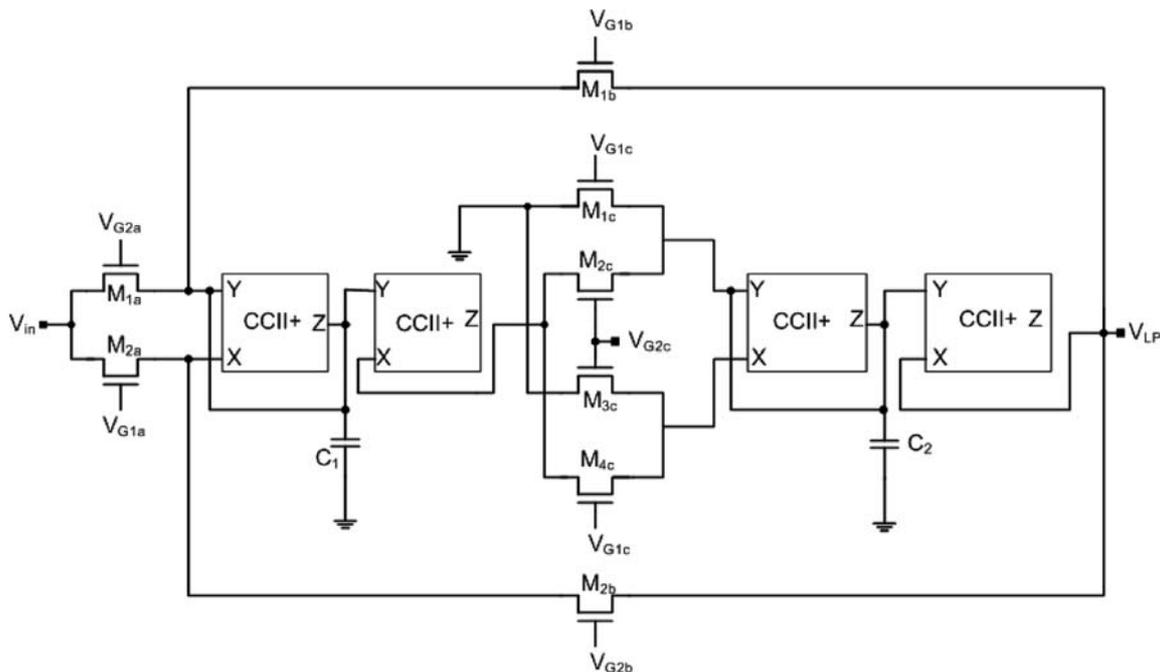
Fig. 12 The second-order MOS-C maximally flat low pass filter based on the proposed CCII +
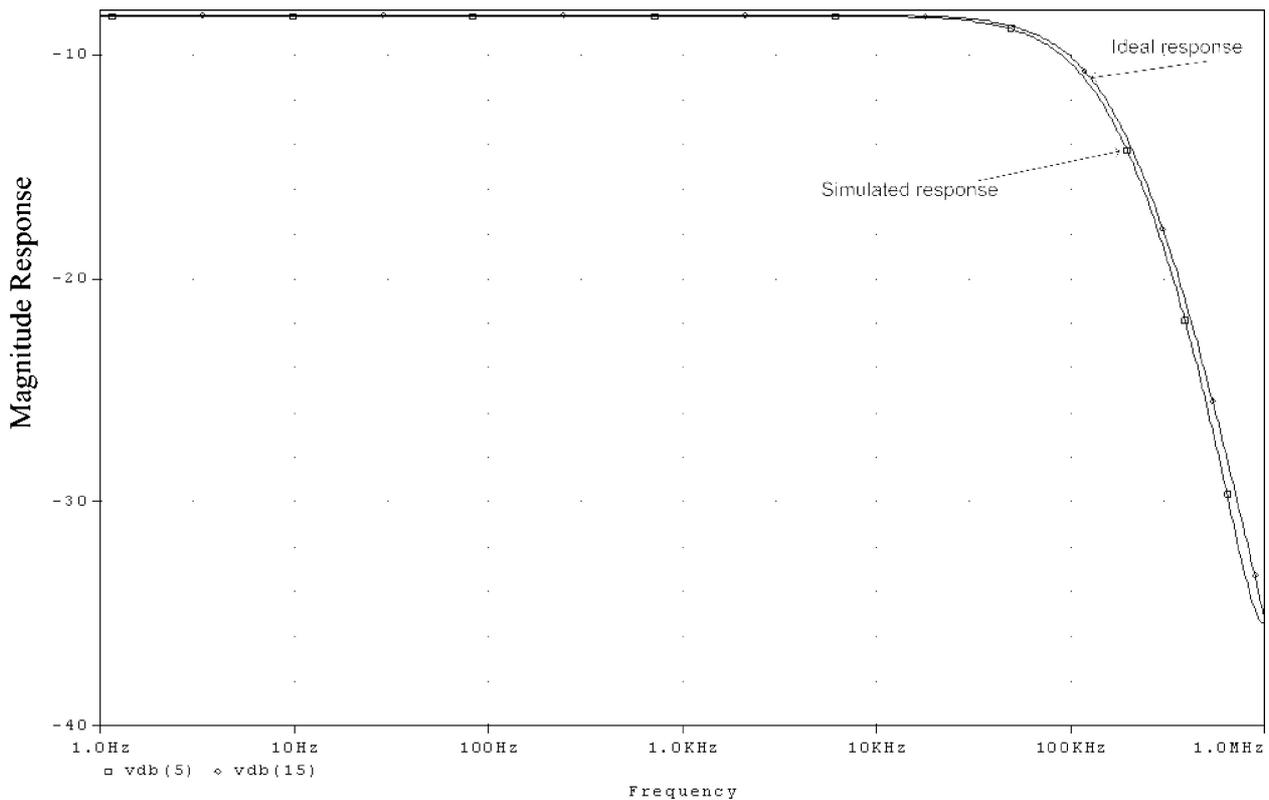
Fig. 13 The ideal and simulated magnitude response of the second order MOS-C maximally flat low pass filter

$$G_b = G_c = G, \quad \text{and} \quad C_1 = C_2 = C \tag{23}$$

Therefore,

$$\omega_O = \frac{G}{C}, \quad \text{and} \quad Q = \frac{G}{(G - G_a)} \tag{24}$$

Figure 13 shows the ideal and simulated magnitude responses of the MOS-C second order maximally flat low-pass filter. The second order MOS-C maximally flat low-pass filter provides a bandwidth of 100 KHz. Also, the input referred noise of the filter circuit found to be less than 30 nV/$\sqrt{\text{Hz}}$.

5 Conclusion

A new CMOS CCII+ was presented, analyzed and simulated. The proposed CCII+ is based on two matched *n*-differential pairs instead of the conventional complementary differential pairs input stage to provide a rail-to-rail input-output range. This CCII+ has reduced the number of current mirrors required in the input stage and this improves the input stage open-loop bandwidth and reduced the voltage transfer error. The CCII+ block is suitable for low-voltage, low-power applications and characterized by the ability to achieve small voltage, current transfer errors and high output driving current capability. Simulation results and a fair simulation comparison between the proposed CCII+ and the CCII+ presented in [26] were given. An application example in designing a MOS-C second-order maximally flat low-pass filter is also provided and simulation results were given.

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