

NEW CMOS Fully Differential Transconductor and Its Application

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Abstract

In this paper, a new technique for linearizing long tail differential pair (LTP) is proposed. It is shown that the proposed linearized fully differential transconductor offers excellent linearity. The proposed transconductor is used to design fully differential second order lowpass and bandpass filters suitable for VLSI. PSpice simulation results for the proposed fully differential transconductor and its filter application indicating the linearity range and verifying the analytical results are also given.

Keywords

Transconductor, filter.

I. INTRODUCTION

Transconductance elements are useful building blocks in analog signal processing systems especially in continuous-time filters and four quadrant multipliers [1]-[8]. Many implementations have been reported in the literature in order to obtain highly linear transconductors. Among these realizations are the one that are based on the long tail differential pair (LTP), which have received a great interest since they offer a relatively low level of distortion because of the negligible second-order effects (mainly body-effect and mobility degradation). In addition, the power consumption of these structures is usually limited compared with other realizations. In the literature, several techniques have been described in order to extend the linearity range of the LTP [1]-[4]. The cross-coupled technique has been first proposed by Khorramabadi [1] by properly scaling the aspect ratios of the differential pair and the bias current used. Then the adaptively biased CMOS differential pair has been introduced by Nedungadi [2]. Recently, Kimura has proposed the dynamic bias current technique [3]. Other techniques have been reported in the literatures [5]-[8]. In this paper, a new CMOS realization of a fully differential transconductor based on transistors operating in the saturation region is given. The transconductor, whose symbol is shown in Figure 1, has two input voltages and provides two output currents through the two output terminals. The structure of the proposed transconductor is based on the current linearization of the long tail differential pair (LTP) by generating suitable biasing currents in term of the differential input voltage to bias the source of the differential pair. As a result, improved linearity of the developed transconductor over the tuning range is obtained. PSpice simulations show that with ± 1.5 V power supply, linearity range is between -0.7 V and 0.7 V. In Section II, The realization of the CMOS fully differential transconductor is presented. In section III, the proposed transconductor is used to design fully differential second order lowpass and bandpass filters. Finally, conclusion is stated in section IV.

II. THE PROPOSED FULLY DIFFERENTIAL TRANSCONDUCTOR CIRCUIT

The proposed fully differential transconductor circuit is shown in Figure 2. The matched transistors M9 and M12 form the basic differential pair and their gate voltages are the input voltages to the transconductor. Each of the two identical circuits formed from M1-M7 and M15-M21 is an equivalent MOSFET cell based on adaptively biased technique which has square law characteristics and whose equivalent threshold voltage can be configured in technology-independent fashion [9]. The remaining transistors M10, M13 perform the current transfer to the source of the differential pair. All the transistors are assumed to be operating in the saturation region with their sources connected to their substrate. The MOS drain current in the saturation region is given by:

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \quad (1)$$

where $K = \mu C_{ox} (W/L)$ is the transconductance parameter of M9 and M12, W/L is the transistor aspect ratio, μ is the electron mobility and C_{ox} is the gate oxide capacitance per unit area. From Figure 2, the output current can be obtained as follows:

$$I_o = I_{o1} - I_{o2} = \sqrt{KI_{SS}} (V_1 - V_2) \sqrt{1 - \frac{K(V_1 - V_2)^2}{4I_{SS}}} \quad (2)$$

where $I_{SS} = I_B + I_{C1} + I_{C2}$ is the total bias current, I_B is the uncompensated bias current, I_{C1} and I_{C2} are the compensating bias currents.

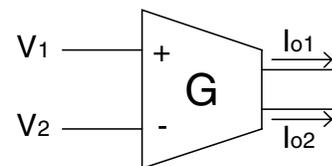


Figure 1. The symbol of the transconductor.

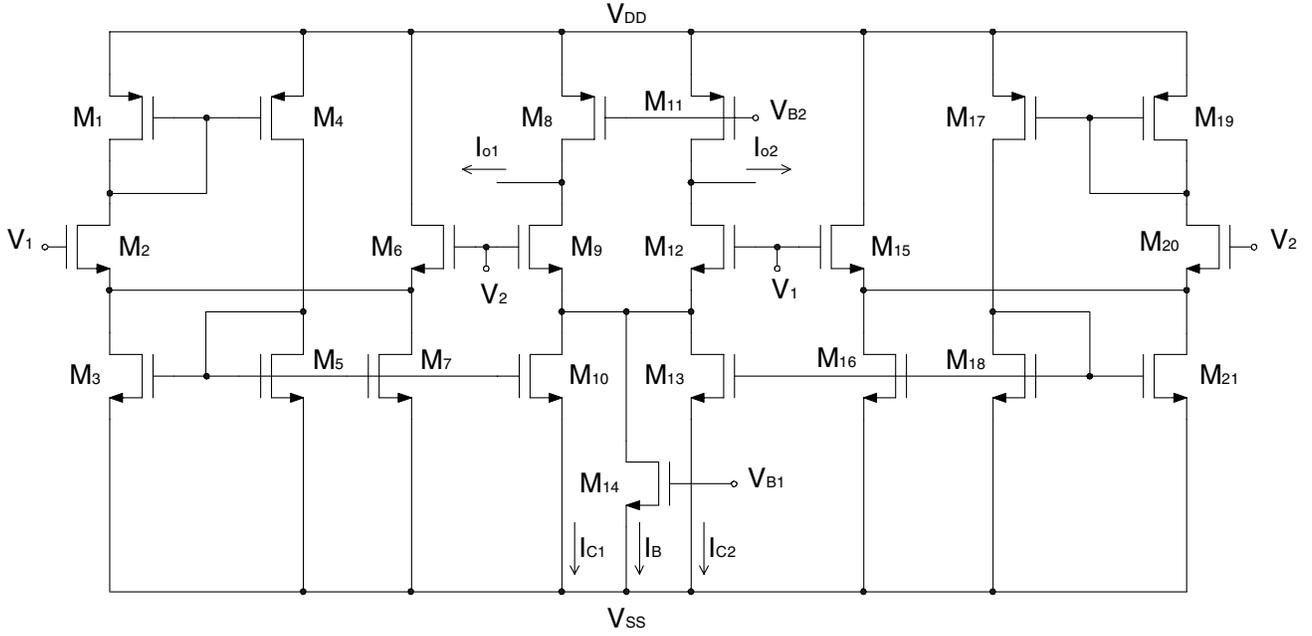


Figure 2. The CMOS circuit of the proposed transconductor.

From the biasing circuit realized from M1-M7 and M10, an expression for the compensating biasing current I_{C1} in terms of V_1 and V_2 was given in [9] by:

$$I_{C1} = \frac{K_2 K_{10}}{2K_5(1-K_\alpha)^2} (V_1 - V_2)^2 \quad (V_1 - V_2) \geq 0 \quad (3)$$

$$\text{where } K_\alpha = \sqrt{\frac{K_2 K_7}{K_5 K_6}}$$

Similarly, an expression for the compensating biasing current I_{C2} can be obtained from the biasing circuit formed from M13 and M15-M21 and is given by:

$$I_{C2} = \frac{K_{13} K_{20}}{2K_{18}(1-K'_\alpha)^2} (V_1 - V_2)^2 \quad (V_1 - V_2) \leq 0 \quad (4)$$

$$\text{where } K'_\alpha = \sqrt{\frac{K_{16} K_{20}}{K_{15} K_{18}}}$$

From the above equations and with the following assumption:

$$\frac{K_2 K_{10}}{K_5(1-K_\alpha)^2} = \frac{K_{13} K_{20}}{K_{18}(1-K'_\alpha)^2} = \frac{K}{2} \quad (5)$$

The total compensating current is given by:

$$I_{C1} + I_{C2} = \frac{K}{4} (V_1 - V_2)^2 \quad (6)$$

From (2) and (6) one gets

$$I_o = I_{o1} - I_{o2} = \sqrt{KI_B} (V_1 - V_2) \quad (7)$$

Therefore, the CMOS circuit shown in Figure 2 operates as a fully differential transconductor with a programmable transconductance G that is given by:

$$G = \sqrt{KI_B} \quad (8)$$

The performance of the proposed transconductor circuit was verified by PSpice simulations using 0.35 μm technology. Supply voltages used are given by: $V_{DD} = -V_{SS} = 1.5\text{V}$, I_B is set to 25 μA . The compensating current ($I_{C1} + I_{C2}$) of the proposed transconductor versus the differential input voltage ($V_1 - V_2$), which is scanned from -0.7 V to 0.7 V, is shown in Figure 3. The differential output current (I_o) of the basic LTP compared with that of the presented transconductor is shown in Figure 4. It's seen that linearity range become wide due to the new linearization technique. The magnitude and phase responses of the transconductor differential output current are shown in Figure 5 with 3-dB frequency 90 MHz. Figure 6 shows the THD of the differential output current of the proposed transconductor and the basic LTP versus input voltage magnitude at 1 MHz. Figure 7 shows the transient response of the differential output current of the

proposed transconductor when a sinusoidal voltage signal of 3 MHz is applied at the input. The output-referred and input-referred noise voltages at 90 MHz for this transconductor when terminated by 1 KΩ are 6 nV and 80 nV, respectively.

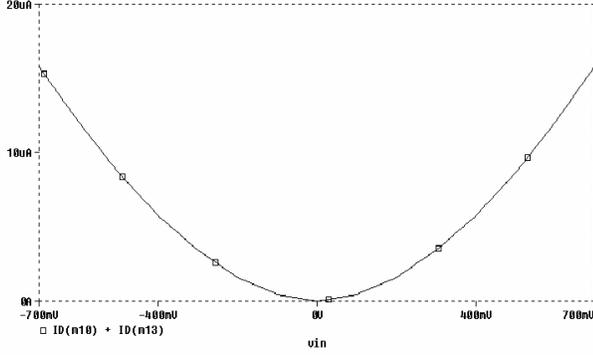


Figure 3. The DC compensating current of the transconductor.

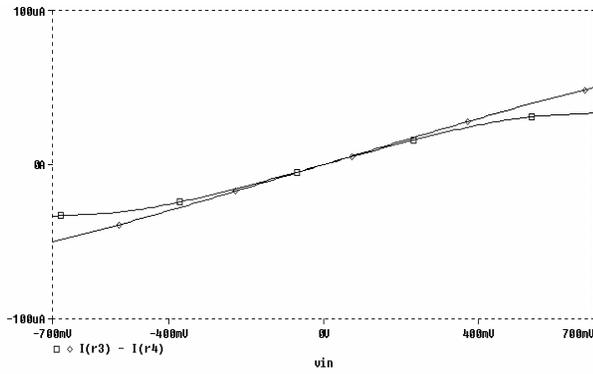


Figure 4. The DC output current of the transconductor and the basic LTP.

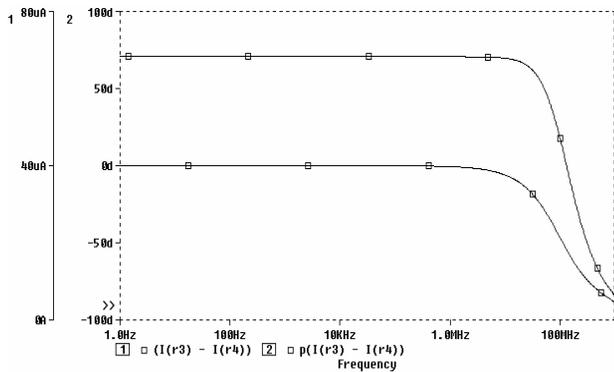


Figure 5. The magnitude and phase responses of the transconductor output current.

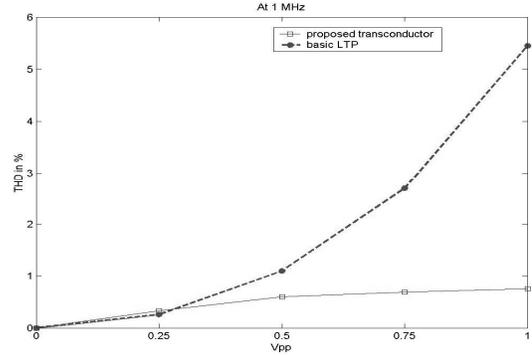


Figure 6. THD of the output current of the transconductor and the basic LTP versus input voltage magnitude at 1 MHz.

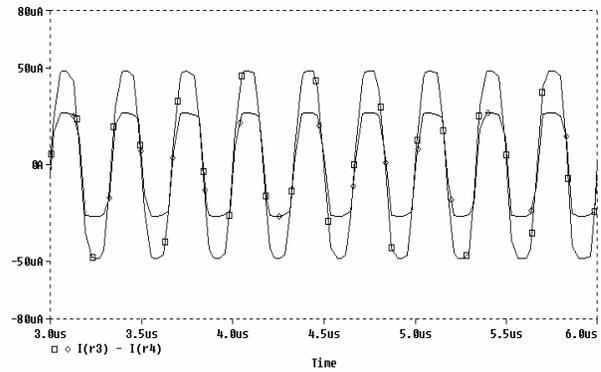


Figure 7. The transient analysis of the output current of the transconductor and the basic LTP.

III. THE FULLY DIFFERENTIAL LOWPASS AND BANDPASS BIQUAD CIRCUIT

Figure 8 represents the filter circuit, which realizes second order lowpass and bandpass functions in a differential form. The circuit includes four transconductors and four grounded capacitors, which makes the filter suitable for VLSI implementation. The transfer functions of the bandpass and the lowpass outputs are given by:

$$\frac{V_{BP}}{V_{id}} = \frac{sG_1/C_1}{D(s)} \quad (9)$$

$$\frac{V_{LP}}{V_{id}} = \frac{(G_1G_2)/(C_1C_2)}{D(s)} \quad (10)$$

where

$$D(s) = s^2 + s \frac{G_3}{C_1} + \frac{G_2G_4}{C_1C_2} \quad (11)$$

$$\omega_o = \sqrt{\frac{G_2G_4}{C_1C_2}} \quad (12)$$

and

$$Q = \frac{\sqrt{G_2 G_4 C_1 / C_2}}{G_3} \quad (13)$$

To simplify the design, let $G_1 = G_2 = G_4 = G$ and $C_1 = C_2 = C$. As a result $\omega_0 = G/C$ and $Q = G/G_3$. Therefore, high Q can be realized by increasing the G/G_3 ratio, which can be achieved by programming G_3 . The PSpice simulation results of the active filter using the proposed transconductor with $G_1 = G_2 = G_4 = G_3/\sqrt{2} = 63 \mu\text{A/V}$ and $C_1 = C_2 = 20 \text{ pF}$ to obtain a maximally flat magnitude lowpass response designed for a DC gain of 1 and $f_o = 500 \text{ KHz}$ is shown in Figure 9(a) indicating the magnitude of the lowpass output. The simulation results of the bandpass response with $G_1 = G_2 = 20G_3 = 315 \mu\text{A/V}$ and $C_1 = C_2 = 20 \text{ pF}$ to obtain a bandpass filter with center frequency $f_o = 2.5 \text{ MHz}$, $Q = 20$ is shown in Figure 9(b) indicating the magnitude of the bandpass output.

IV. CONCLUSION

A new linearization technique for the LTP has been proposed. It has been shown that the proposed circuit is a very attractive solution to overcome the restrictions that limited the use of LTP in many applications. The application of the proposed transconductor to realize fully differential lowpass and bandpass filter is also presented.

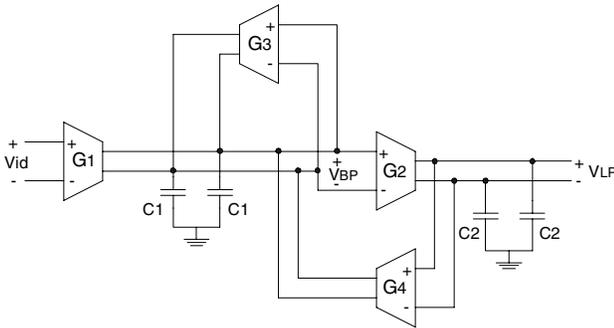


Figure 8. The fully differential bandpass-low pass filter.

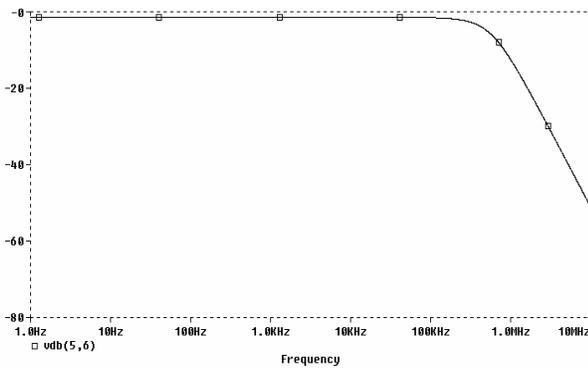


Figure 9(a). The magnitude response of the lowpass filter output.

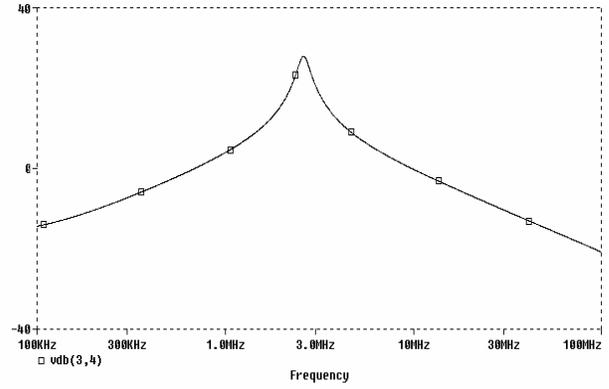


Figure 9(b). The magnitude response of the bandpass filter output.

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