The Differential Difference Operational Floating Amplifier: A New Block for Analog Signal Processing in MOS Technology

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Abstract— A wide-range differential difference operational floating amplifier (DDOFA) is introduced. The DDOFA is a new block useful for continuous-time analog signal processing. The DDOFA is realized using a differential difference transconductor with large signal handling capability and a single input differential output current op-amp. The DDOFA forces two differential voltages to the same value and provides two balanced output currents. This brief presents a CMOS realization of the DDOFA, and some of its applications are provided, such as a voltage-to-current converter, MOS-grounded and floating resistors, a MOS multiplier/divider cell, a differential integrator, a continuous-time MOS-C filter, a MOS-C current oscillator, and a MOS-C floating inductor. Simulation results for the DDOFA circuit and its applications are given.

Index Terms—Operational floating amplifier.

I. INTRODUCTION

Before discussing the differential difference operational floating amplifier, a short refresher of the differential difference amplifier (DDA) is given. As discussed in [1]–[5], the DDA, whose symbol is shown in Fig. 1, is an extension of the concept of the op-amp, the main difference being that, instead of two single-ended inputs as in the case of op-amps, it has two differential input ports $(V_2 - V_1)$ and $(V_4 - V_3)$. The output voltage of the DDA can be written as

$$V_o = A_o[(V_2 - V_1) - (V_4 - V_3)] \qquad (1)$$

where A_o is the open-loop gain of the DDA. When a negative feedback is introduced to V_1 and/or V_4, the basic equation that characterizes the operation of the DDA is obtained as

$$V_2 - V_1 = V_4 - V_3 \qquad \text{with } A_o \to \infty. \qquad (2)$$

The DDOFA, whose symbol is shown in Fig. 2, also has two differential input ports, but in addition, it provides two balanced output currents through the two output terminals instead of one output voltage as in the cases of op-amps and DDA's. Therefore, the output currents of the DDOFA can be written as

$$I_{o+} = -I_{o-} = G_o[(V_2 - V_1) - (V_4 - V_3)] \qquad (3)$$

where G_o is the open-loop transconductance gain of the DDOFA. If a negative feedback is introduced, from I_{o+} (I_{o-}) to V_1 and/or V_4 $(V_2$ and/or $V_3)$ which is indicated from (3), the following expression is obtained:

$$V_2 - V_1 = V_4 - V_3 \qquad \text{with } G_o \to \infty. \qquad (4)$$
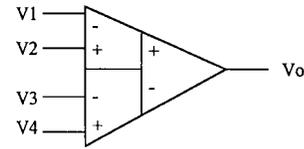
Fig. 1. Symbol for the DDA.
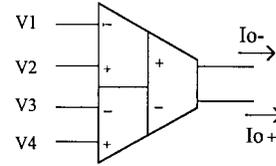
Fig. 2. Proposed symbol for the DDOFA.

For a finite open-loop transconductance gain G_o, the difference between the two differential voltages increases as G_o decreases. Therefore, the open-loop transconductance gain should be as large as possible to achieve high-performance operation. The DDOFA is realized using a differential difference transconductor which converts the two differential voltages into a current which is then amplified by using current op-amps with balanced outputs.

In this brief, an NMOS realization of a programmable linear differential difference transconductor with large signal-handling capability is given in Section II. In Section III, the overall DDOFA circuit using the proposed differential difference transconductor and current op-amp is given. Specific DDOFA-based applications, such as a voltage-to-current converter, a MOS grounded resistor, a MOS floating resistor, a MOS multiplier/divider cell, and the application of the DDOFA in the realization of a continuous-time MOS-C filter, a MOS-C current oscillator, and a MOS-C floating inductor are given in Section IV. Simulation results using PSPICE for the DDOFA circuit and its applications which verify the analytical results are also provided after each application.

II. THE PROPOSED DIFFERENTIAL DIFFERENCE TRANSCONDUCTOR

In this section, a realization of a linear NMOS differential difference transconductor whose transconductance can be tuned by a bias voltage V_B is introduced. The differential difference transconductor represents the input stage of the DDOFA shown in Fig. 3 and is formed from transistors $M1$–$M16$. All transistors are assumed to be operating in the saturation region with their sources connected to their substrates.

The drain current of the NMOS transistor in that region is given by

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \qquad (5)$$

where $K = \mu_n C_{ox}(W/L)$, (W/L) is the transistor aspect ratio, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, and V_T is the threshold voltage (assumed to be the same for every NMOS transistor).

Transistors $M1$–$M8$ are assumed to be matched transistors, and their currents are linearized by using the four biasing circuits formed from transistors $M9$–$M16$. First, expressions for the biasing voltages V_a, V_b, V_c, and V_d in terms of V_1, V_2, V_3, and V_4, respectively, are obtained.
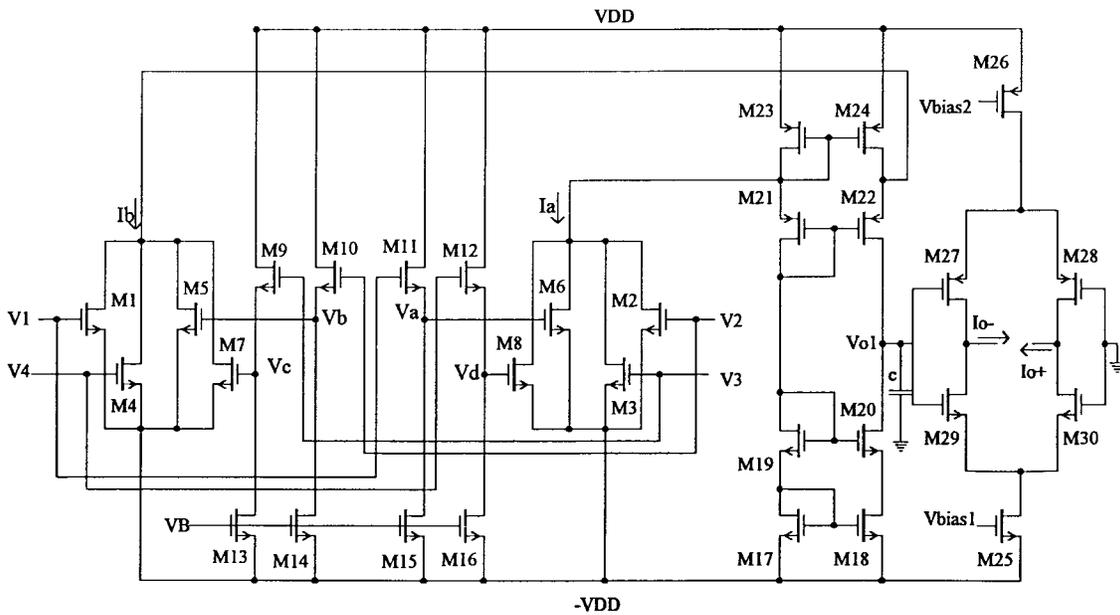
Fig. 3.   Overall DDOFA circuit.
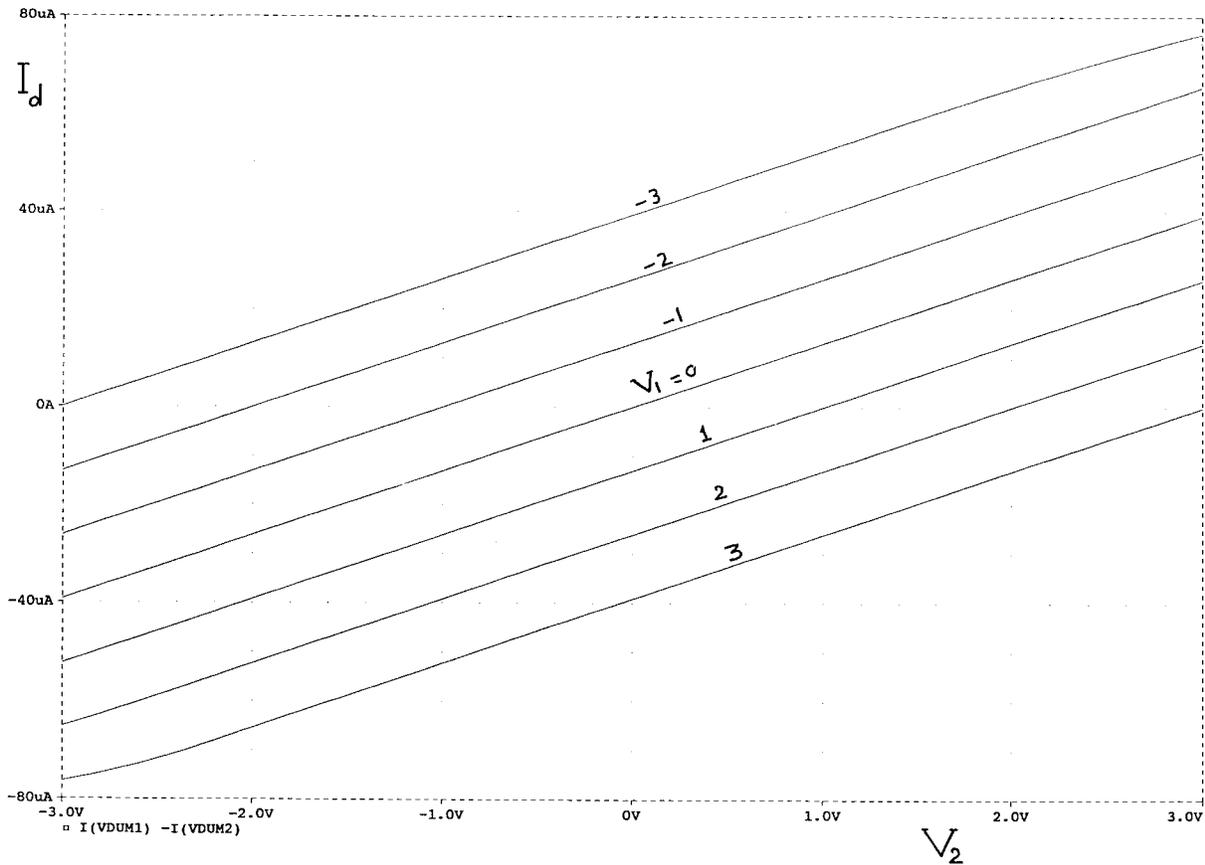
Fig. 4.   Differential current I_d of the differential difference transconductor when the inputs of the same polarity are shorted together.

Consider the biasing circuit formed from $M11$ and $M15$; the current flowing through M11 is given by

$$I_{11} = \frac{K_{11}}{2}(V_1 - V_a - V_T)^2 \qquad (6)$$

and the same current flowing through $M15$ is given by

$$I_{15} = \frac{K_{15}}{2}(V_B + V_{DD} + V_T)^2 \qquad (7)$$

where V_B is the control voltage, taking, $K_{11} = K_{15}$; hence, from (6) and (7), the biasing voltage V_a is given by

$$V_a = V_1 - V_B - V_{DD}. \tag{8}$$

Similar expressions for the biasing voltages V_b, V_c, and V_d can be obtained and are given, respectively, by

$$V_b = V_2 - V_B - V_{DD} \tag{9}$$
$$V_c = V_3 - V_B - V_{DD} \tag{10}$$
$$V_d = V_4 - V_B - V_{DD}. \tag{11}$$

Therefore, the currents flowing through $M1$–$M8$ can be obtained. The current of the transistors $M1$–$M4$ can be written as

$$I_i = \frac{K}{2}(V_i - V_{DD} - V_T)^2, \quad \text{for } i = 1, 2, 3, 4. \tag{12}$$

The currents of the transistors $M5$–$M8$ are given, respectively, by

$$I_5 = \frac{K}{2}(V_2 - V_B - V_T)^2 \tag{13}$$
$$I_6 = \frac{K}{2}(V_1 - V_B - V_T)^2 \tag{14}$$
$$I_7 = \frac{K}{2}(V_3 - V_B - V_T)^2 \tag{15}$$
$$I_8 = \frac{K}{2}(V_4 - V_B - V_T)^2. \tag{16}$$

The transconductance output current I_d is given by

$$I_d = I_a - I_b. \tag{17}$$

From Fig. 3

$$I_d = (I_2 + I_3 + I_6 + I_8) - (I_1 + I_4 + I_5 + I_7). \tag{18}$$

By substituting from (12)–(16) in (18), the transconductor output current I_d is given as

$$I_d = G_m[(V_2 - V_1) - (V_4 - V_3)] \tag{19}$$

where

$$G_m = K(V_B + V_{DD}). \tag{20}$$

Therefore, the NMOS circuit formed from transistors $M1$–$M16$ and shown in Fig. 3 operates as a differential difference transconductor with a programmable transconductance G_m.

Fig. 4 shows the PSPICE simulation results of the differential current of the differential difference transconductor indicating the wide linearity range when V_1 and V_4 are shorted and V_2 and V_3 are also shorted and scanned from -3 to 3 V with $V_B = -3.7$ V and the supply voltage $V_{DD} = 5$ V. The THD of the 1 V peak-to-peak 100 kHz sinusoidal input signal of the differential difference transconductor is 0.498%.

III. THE OVERALL DDOFA CIRCUIT

The overall DDOFA circuit using the differential difference transconductor is shown in Fig. 3. The two output currents of the
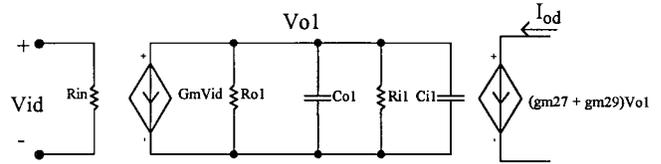
Fig. 5. Simplified function model for the DDOFA.
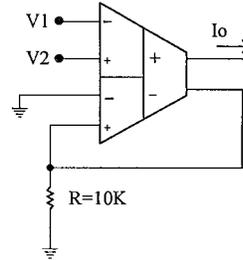
Fig. 6. DDOFA-based voltage-to-current converter.

transconductor I_a and I_b are subtracted and converted into a voltage with a high gain by using the complementary folded cascode amplifier formed from transistors $M17$–$M24$ [6]. The amplified voltage is then converted into two balanced currents I_{o+} and I_{o-} by using the transconductance output stage formed from $M25$–$M30$ [7]–[11]. In addition, a compensation capacitor (C) is added between the V_{o1} node and ground.

A simplified function model for the DDOFA can be introduced as in the case of the op-amp [12] which is composed of ideal circuit elements shown in Fig. 5. The input signal is the differential difference voltage $V_{id} = (V_2 - V_1) - (V_4 - V_3)$ applied across R_{in} (considered to be infinity). This voltage is converted into a current $G_m V_{id}$, where G_m is the transconductance of the differential difference transconductor circuit. This current is converted into a voltage V_{o1} by the gain stage of equivalent output resistance and capacitance R_{o1} and C_{o1}, respectively. This voltage is then converted into two balanced currents I_{o+} and I_{o-} by the output transconductor with the equivalent input resistance and capacitance R_{i1} (considered to be infinity) and C_{i1} (includes the compensating capacitor). The frequency-dependent output current of the DDOFA is given by

$$I_{o+} = \frac{G_o \omega_P}{S + \omega_P}[(V_2 - V_1) - (V_4 - V_3)] \tag{21}$$

where the open-loop gain G_o is given by

$$G_o = \tfrac{1}{2}G_m\{[g_{m20}r_{ds20}r_{ds18}]//[g_{m22}r_{ds22}r_{ds24}]\}$$
$$\cdot (g_{m27} + g_{m29}) \tag{22}$$

and ω_P is given by

$$\omega_P = \frac{1}{\{[g_{m20}r_{ds20}r_{ds18}]//[g_{m22}r_{ds22}r_{ds24}]\}(C_{o1}//C_{i1})} \tag{23}$$

where G_m is the transconductance of the differential difference transconductor.

PSPICE simulation results for the DDOFA circuit are given in Table I, with the transistor aspect ratios given in Table II, and the compensation capacitor $C = 5$ pF.
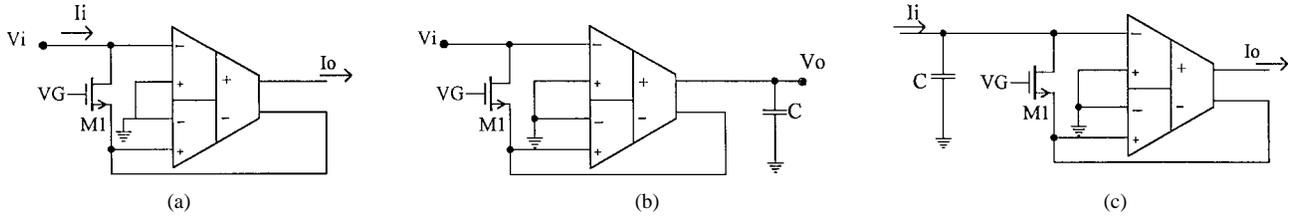
Fig. 7. (a) DDOFA-based grounded resistor. (b) Noninverting integrator using the DDOFA grounded resistor. (c) Lossy current integrator using the DDOFA grounded resistor.

TABLE I

The supply voltage	$V_{DD} = 5$V
The control voltage	$V_B = -3.7$V

Parameters	Simulation results
Standby DC power dissipation	10mW
Input offest voltage	1mV
DC gain	50 Db mA/V
Unity gain BW	10MHz
Phase margin	60 degree
Common mode input	-3.5 to 3.5 V

TABLE II

MOS Transistor	Aspect ratio (W μm / L μm)
M1-M8	2/16
M9-M16	4 / 4
M17,M24	160/10
M25-M30	30/2

IV. APPLICATIONS OF THE DDOFA

In the following subsections, several applications of the DDOFA circuit are discussed, and the PSPICE simulation results are given to verify the concepts.

A. The DDOFA Voltage-to-Current Converter

Fig. 6 shows the DDOFA differential voltage-to-current converter. The voltage-to-current converter has a high input impedance since the inputs of this circuit are directly the inputs of the DDOFA's (gates of MOS transistors). In addition, only a single grounded resistor is needed. The output current of this circuit is given by

$$I_o = \frac{(V_1 - V_2)}{R}. \tag{24}$$

PSPICE simulations of the voltage-to-current converter stepping V_2 from -1.5 to 1.5 V in steps of 0.75 V sweeping V_1 from -1.5 to 1.5 V (similar to what has been shown in Fig. 4) reveals a linear current variation of ± 140 μA. The THD of a 100-kHz input signal with 1 V peak-to-peak is 0.439%.

B. DDOFA-MOS Grounded and Floating Resistors

An equivalent grounded and floating resistor can be realized using the DDOFA and MOS transistors operating in the nonsaturation region. The current through the MOS transistors in that region can be linearized if its drain and its source are out of phase [13].

1) The MOS Grounded Resistor: The DDOFA-MOS grounded resistor is shown in Fig. 7(a), where the DDOFA inverter is connected between the drain and the source nodes of the transistor. Therefore, the input current of the circuit equals the linearized drain current of
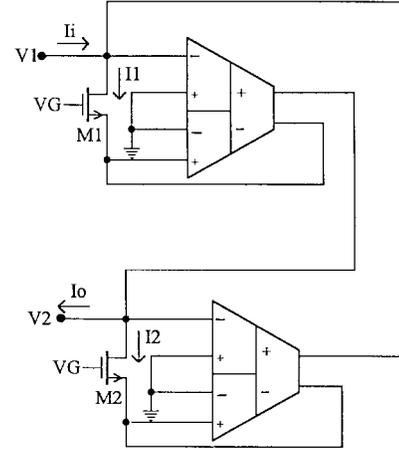
Fig. 8. DDOFA-based floating resistor.

the MOS transistor M_1 which is given by

$$I_i = 2K(V_G - V_T)V_i, \qquad \text{for } V_G \geq |V_i| + V_T. \tag{25}$$

Therefore, the circuit is equivalent to a voltage-controlled grounded resistor with magnitude given by

$$R = \frac{1}{2K(V_G - V_T)}. \tag{26}$$

PSPICE simulations of the MOS grounded resistor stepping V_G from 2.5 to 4.5 V in steps of 0.5 V sweeping V_i from -1 to 1 V reveals a linear characteristic, and for a 1-V peak-to-peak 100-kHz input signal the THD calculated using $V_G = 3$ V and $K = 55/3$ μA/V^2 is 0.589%.

The circuit shown in Fig. 7(a) also realizes a voltage-to-current converter by using the extra output terminal of the DDOFA. The output current I_o is given by

$$I_o = I_i = 2K(V_G - V_T)V_i. \tag{27}$$

A noninverting integrator can be realized as shown in Fig. 7(b), and the output voltage V_o is given by

$$V_o = \frac{2K(V_G - V_T)}{SC}V_i. \tag{28}$$

A lossy current integrator is realized as shown in Fig. 7(c), and the output current I_o is given by

$$I_o = \frac{1}{1 + \dfrac{SC}{2K(V_G - V_T)}}I_i. \tag{29}$$

(a)

(b)
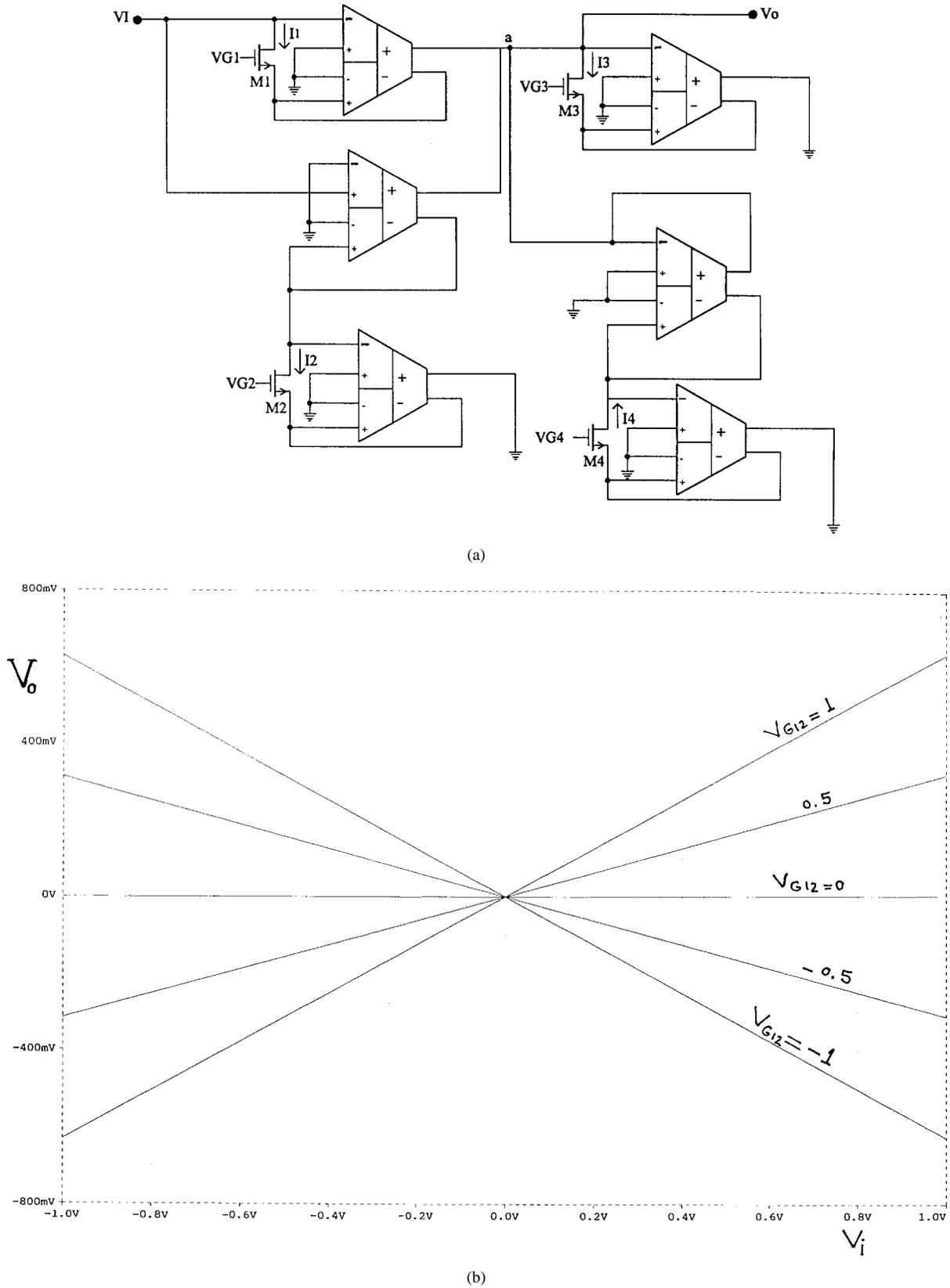
Fig. 9. (a) DDOFA-based multiplier/divider cell. (b) DC curves of the multiplier.

2) The MOS Floating Resistor: The DDOFA can also be used to realize a floating resistor as shown in Fig. 8, where $M1$ and $M2$ are matched transistors operating in the nonsaturation region. The input and output currents of the floating resistor are forced to be the difference between the linearized currents I_1 and I_2. Therefore,

$$I_i = I_o = I_1 - I_2 = 2K(V_G - V_T)(V_1 - V_2). \qquad (30)$$
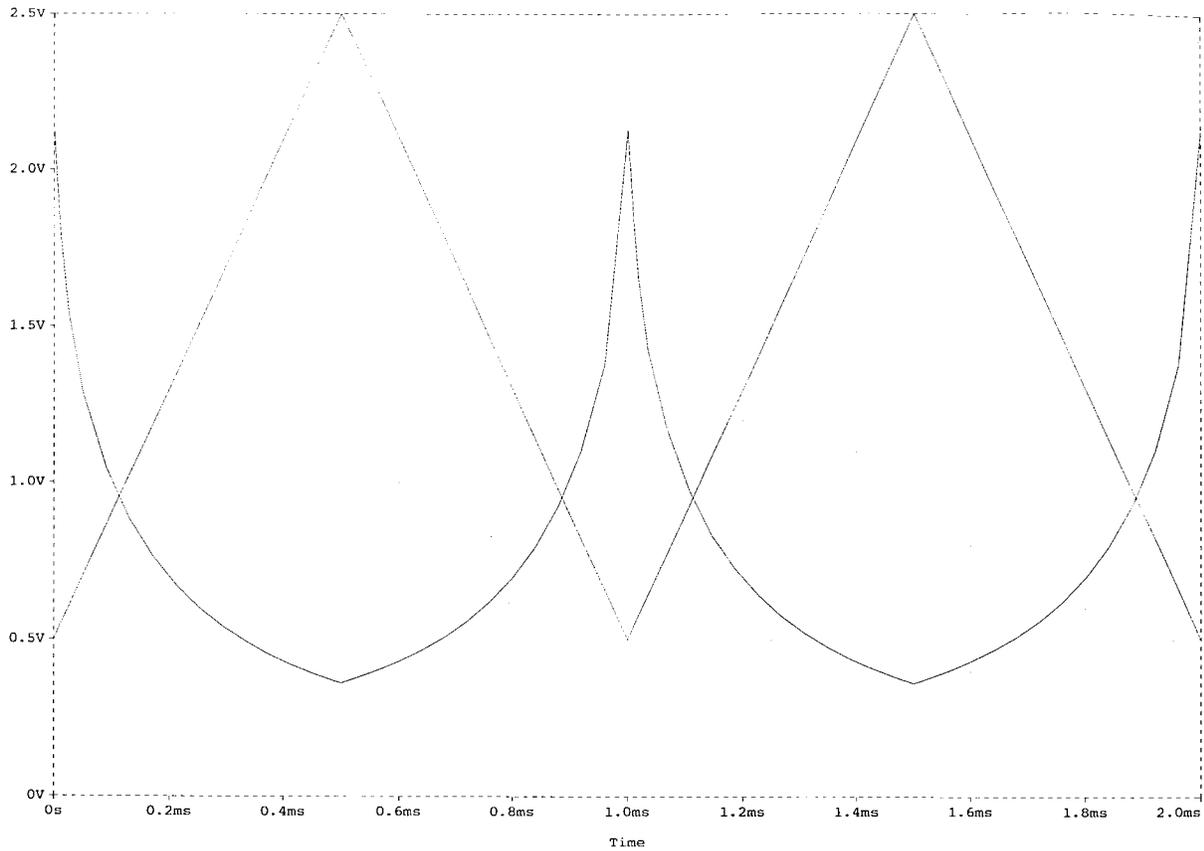
Fig. 9. (*Continued.*) (c) Output voltage of the divider along with the triangle input signal.

Therefore, the circuit shown in Fig. 8 is equivalent to a voltage-controlled floating resistor with magnitude given by

$$R = \frac{V_1 - V_2}{I_i} = \frac{1}{2K(V_G - V_T)}. \qquad (31)$$

PSPICE simulations of the MOS grounded resistor stepping V_2 from -1 to 1 V in steps of 0.5 V sweeping V_1 from -1 to 1 V (similar to what has been shown in Fig. 4), reveals a linear current variation of ± 60 μA and for a 1-V peak-to-peak 100-kHz input signal, the THD calculated using $V_G = 3$ V and $K = 55/3$ μA/V^2 is 0.589%.

C. The DDOFA–MOS Multipler/Divider Cell

Analog multipliers and dividers have a wide range of applications in traditional analog signal processing, telecommunications, and electronic systems, as well as in analog computational systems based on biological neural paradigms [13]–[18].

A MOS multiplier/divider cell can be realized using the DDOFA and MOS transistors operating in the nonsaturation region by using circuit techniques similar to that used in obtaining linear grounded and floating resistors. The proposed MOS multiplier/divider circuit is shown in Fig. 9(a). It comprises six DDOFA's and four MOS transistors operating in the nonsaturation region, where $M1$ and $M2$ are matched transistors, and $M3$ and $M4$ are also matched transistors. The cell is reconfigurable to achive a four-quadrant multiplicative or division through the same topology with no additional circuitry. The output voltage of the circuit is tunable via gate control voltages. The current differences of the MOS transistors $M1$, $M2$, and the MOS

transistors $M3$, $M4$ are given, respectively, by

$$I_1 - I_2 = 2K_i(V_{G1} - V_{G2})V_i \qquad (32)$$

$$I_3 - I_4 = 2K_o(V_{G3} - V_{G4})V_o. \qquad (33)$$

Applying the KCL at node a, one obtains

$$V_o = \frac{K_i}{K_o} \frac{(V_{G1} - V_{G2})}{(V_{G3} - V_{G4})} V_i. \qquad (34)$$

Thus, the circuit achieves the computation of $(\Delta V_{G12}/\Delta V_{G34})V_i$. The circuit also performs four-quadrant multiplication for the input signals V_i and $(V_{G1} - V_{G2})$ with the gate voltages V_{G3} and V_{G4} as the control voltages. The circuit also operates as a divider circuit for the input signals V_i and $(V_{G3} - V_{G4})$ with the gate voltages V_{G1} and V_{G2} as the control voltages.

The dc transfer curves of the circuit as a multiplier are shown in Fig. 9(b) with V_i scanned from -1 to 1 V and the differential gate voltage $(V_{G1} - V_{G2})$ scanned from -1 to 1 V . The THD for a 1-V peak-to-peak 100-kHz input signal is 0.604%. The circuit is also tested as a divider in which the process of signal inversion is demonstrated. In this application, the V_i and V_{G12} are held constant, $V_i = 1$ V, $V_{G1} = 4$ V, $V_{G2} = 3$ V, V_{G34} is a 1-kHz triangular wave varying between 0.5 and 2.5 V, $K_i = 25$ μA/V^2 and $K_o = 55/2$ μA/V^2. The output voltage V_o which is proportional to $1/V_{G34}$ is shown in Fig. 9(c), along with the input signal V_i.

D. The DDOFA-Based Differential Integrator

Fig. 10(a) shows the DDOFA-based differential integrator. The DDOFA differential integrator has a high input impedance since the inputs of the circuit are directly the inputs of the DDOFA's (gates

(a)

(b)
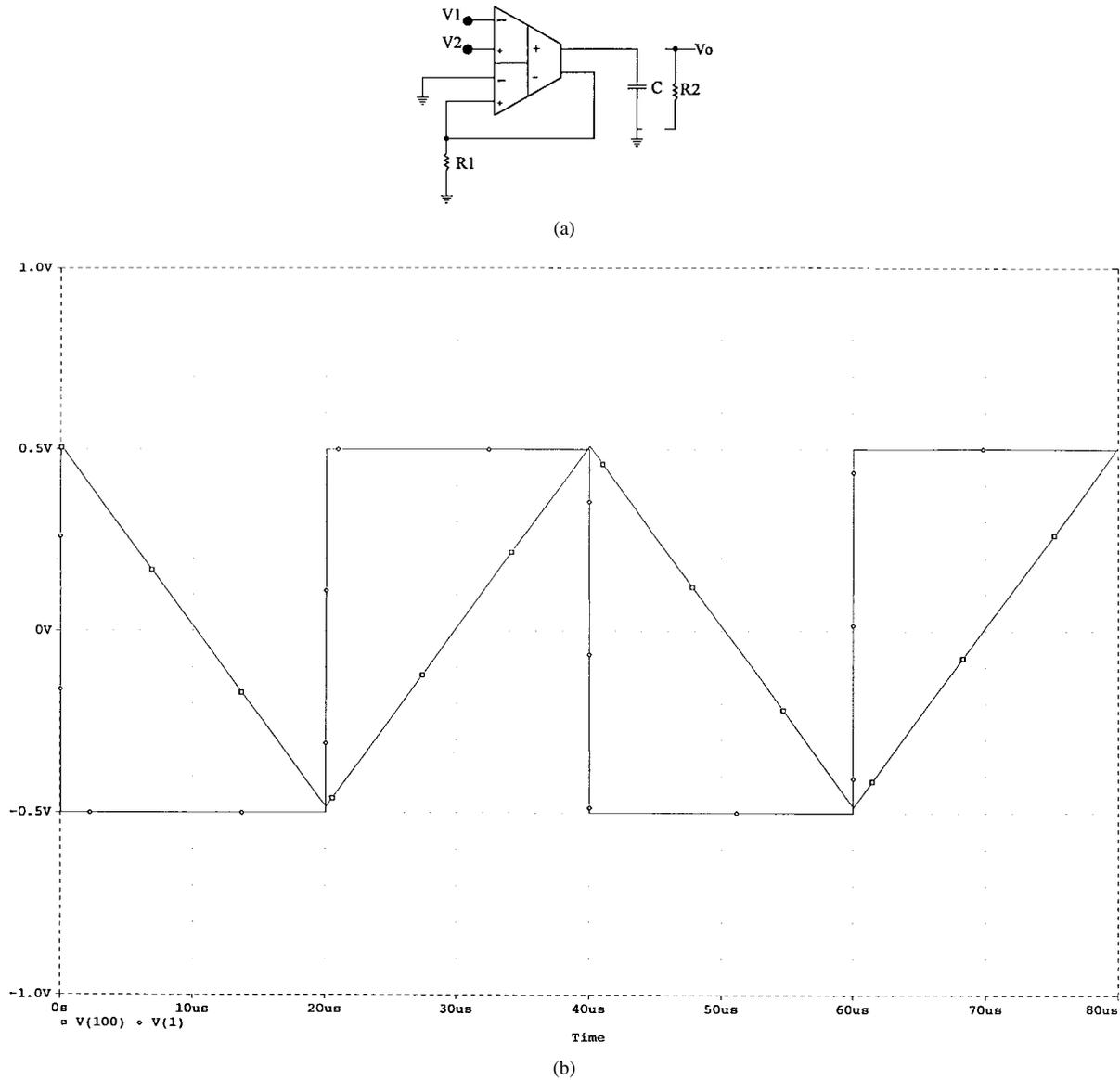
Fig. 10.　(a) DDOFA-based differential integrator. (b) Output of the integrator along with the square wave input signal.

of MOS transistors). In addition, only a single grounded resistor and a single grounded capacitor are needed; hence, there are no passive component-matching requirements. The output of the circuit without R_2 is given by

$$V_o = \frac{V_1 - V_2}{SCR_1}. \tag{35}$$

Fig. 10(b) shows the PSPICE simulation results of the integrator with a square-wave input of 1 V amplitude and a frequency of 25 kHz, where $R = 10$ kΩ and $C = 1$ nF. By adding the grounded resistor R_2 in parallel with the capacitor, a lossy integrator can be obtained with an output voltage given by

$$V_o = \frac{1/R_1 C}{S + 1/R_2 C}(V_1 - V_2). \tag{36}$$

E. The DDOFA-MOS-C Continuous Time Filter

The differential integrator is a basic building block in realizing continuous-time filters [20]–[25]. The DDOFA-based differential integrator and the DDOFA-based grounded resistor are used to implement a continuous-time filter with voltage and current outputs for both the bandpass and highpass and a voltage output for the lowpass characteristic as shown in Fig. 11(a). The transfer functions of the filter are given by

$$\frac{V_{HP}}{V_I} = \frac{S^2}{D(s)} \tag{37}$$

$$\frac{I_{HP}}{V_I} = \frac{S^2/R_1}{D(s)} \tag{38}$$

$$\frac{V_{BP}}{V_I} = \frac{-S/R_1 C_1}{D(s)} \tag{39}$$

$$\frac{I_{BP}}{V_I} = \frac{-S/R_1 R_2 C_1}{D(s)} \tag{40}$$

$$\frac{V_{LP}}{V_I} = \frac{\frac{1}{R_1 R_2 C_1 C_2}}{D(s)} \tag{41}$$

(a)

(b)
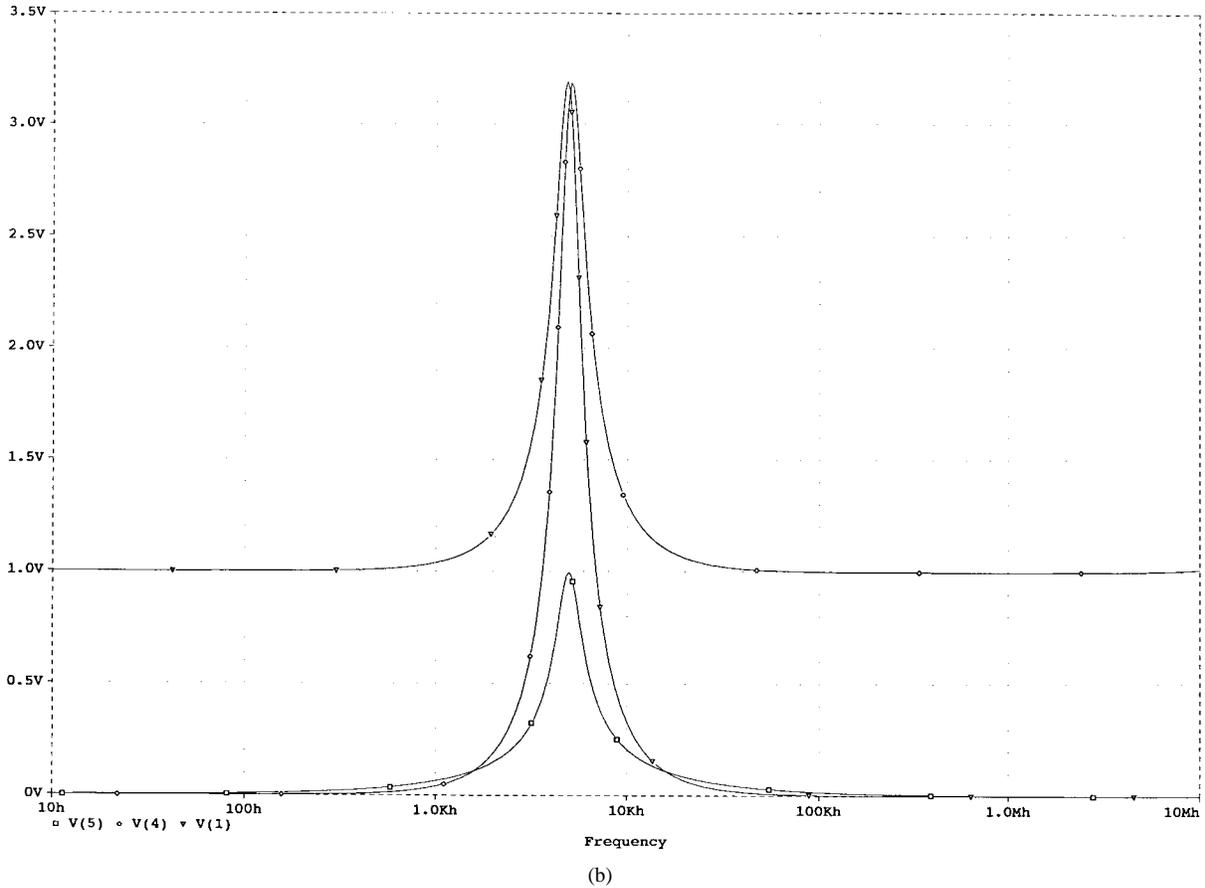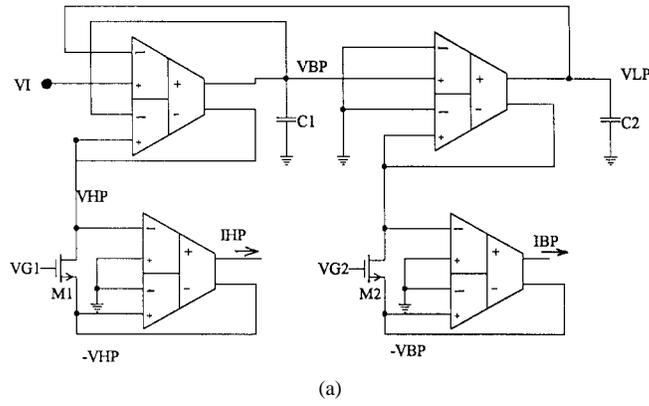
Fig. 11.   (a) DDOFA-based MOS-C continuous-time filter. (b) LP, BP, and HP responses.

where

$$D(S) = S^2 + \frac{1}{R_1 C_1} S + \frac{1}{R_1 R_2 C_1 C_2}$$

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \quad \text{and} \quad Q = \sqrt{\frac{R_1 C_1}{R_2 C_2}}. \qquad (42)$$

The magnitudes of R_1 and R_2 are given by

$$R_1 = \frac{1}{2 K_1 (V_{G1} - V_T)}, \quad R_2 = \frac{1}{2 K_2 (V_{G2} - V_T)}. \qquad (43)$$

The PSPICE simulation results for the LP, BP, and HP characteristics are shown in Fig. 11(b), where $R_1 = 10 \,\text{k}\Omega, R_2 = 10 \,\text{k}\Omega, K_1 = K_2 = 25 \,\mu\text{A/V}^2$, $V_{G1} = V_{G2} = 3$ V, $C_1 = 10$ nF, and $C_2 = 1$ nF.

F. The DDOFA-MOS-C Current Oscillator

Fig. 12(a) shows the DDOFA current oscillator. The oscillator has two outputs $I_{\text{osc}1}$ and $I_{\text{osc}2}$. In this circuit, a new block is introduced which makes the node voltages and currents of a and b out of phase. In addition to this block, two MOS grounded resistors and two capacitors are used to implement the oscillator. The condition of oscillation is given by

$$\frac{R_2}{R_1} + \frac{C_1}{C_2} = 1. \qquad (44)$$

Taking

$$\frac{R_2}{R_1} = \frac{C_1}{C_2} = \frac{1}{2} \qquad (45)$$

(a)

(b)
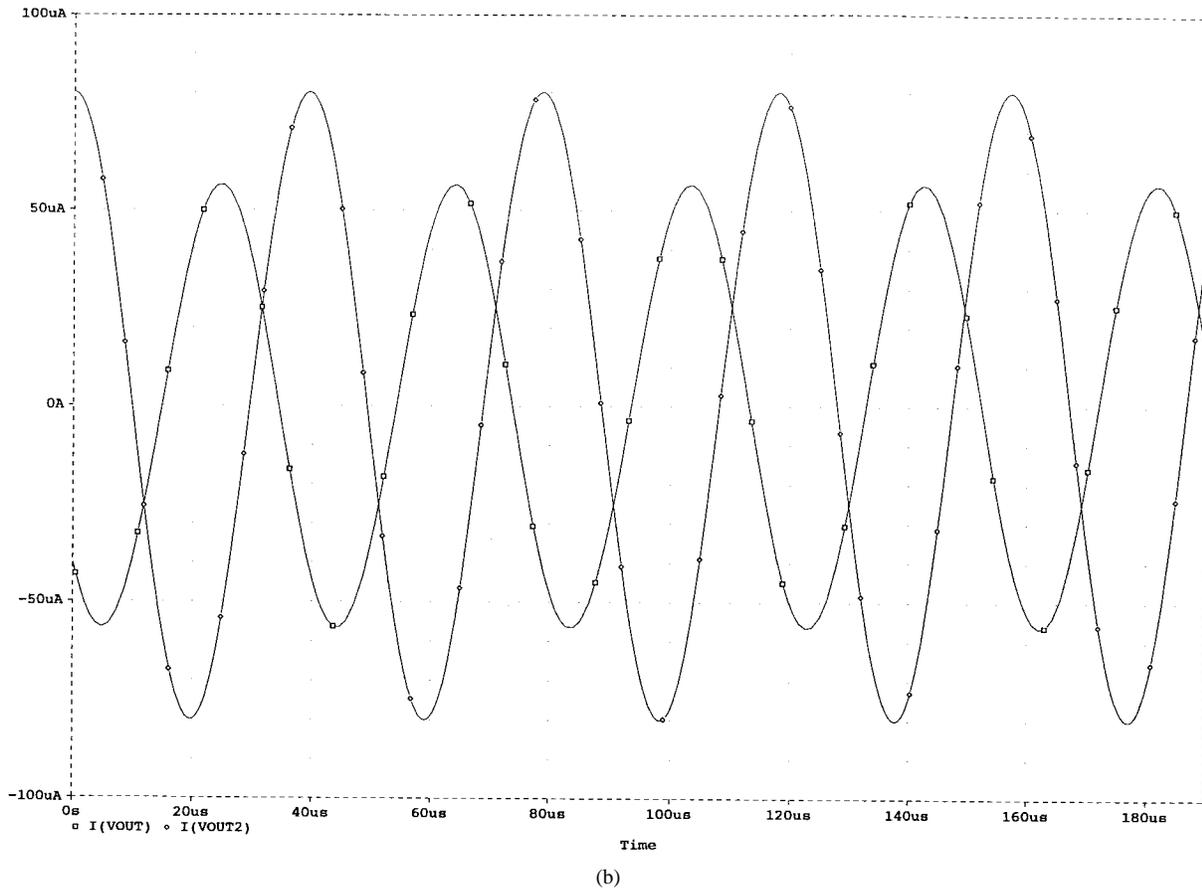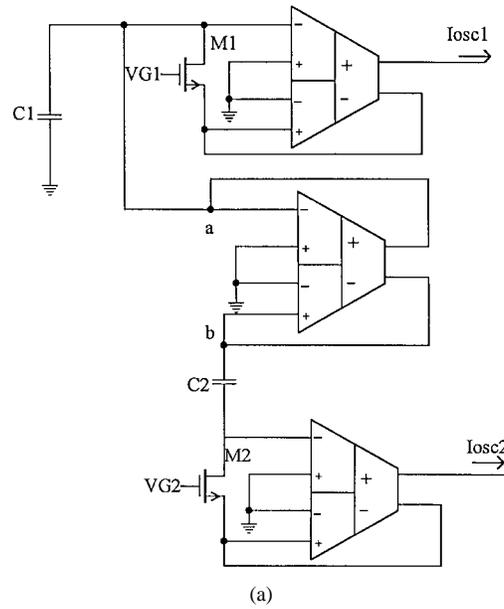
Fig. 12. (a) DDOFA-based MOS-C current oscillator. (b) Two current waveforms of the current oscillator.

the radian frequency of oscillation is given by

$$\omega_{osc} = \frac{1}{R_1 C_1} \qquad (46)$$

where

$$R_1 = \frac{1}{2 K_1 (V_{G1} - V_T)} \quad \text{and} \quad R_2 = \frac{1}{2 K_2 (V_{G2} - V_T)}. \qquad (47)$$

Fig. 12(b) shows the output waveform of the proposed oscillator shown in Fig. 12(a) with the oscillation frequency adjusted to 25 kHz by taking $V_{G1} = V_{G2} = 3$ V, $K_1 = \frac{1}{2} K_2 = \frac{5}{3}$ μA/V^2, and $C_1 = \frac{1}{2} C_2 = 0.5$ nF.

In a practical implementation, the condition of oscillation may not be achived exactly, the tuning property of the voltage-controlled grounded resistors R_1 and R_2 can be used to achieve the condition of oscillation.

TABLE III

No.	DDOFA-based application	Fig.	Basic equations that describe the operation of the application	THD for V_I (P-P) = 1V and f = 100KHz
1	Voltage to Current Converter	6	$I_o = \dfrac{(V_1 - V_2)}{R}$	0.439 %
2	MOS-Grounded Resistor	7(a)	$R = \dfrac{V_i}{I_i} = \dfrac{1}{2K(V_G - V_T)}$	0.598 %
3	MOS-Floating Resistor	8	$R = \dfrac{(V_1 - V_2)}{I_i} = \dfrac{(V_1 - V_2)}{I_o} = \dfrac{1}{2K(V_G - V_T)}$	0.598 %
4	MOS- Multiplier/Divider Cell	9(a)	$V_o = \dfrac{K_i(V_{G1} - V_{G2})}{K_o(V_{G3} - V_{G4})} V_i$	0.604 % (for the multiplier)
5	Lossless Differential Integrator	10(a)	$V_o = \dfrac{(V_1 - V_2)}{SCR_1}$	—
5	Lossy Differential Integrator	10(a)	$V_o = \dfrac{1/R_1 C}{S + 1/R_2 C}(V_1 - V_2)$	—
6	MOS-C Continuous-Time Filter	11(a)	$\dfrac{V_{HP}}{V_I} = \dfrac{S^2}{D(s)} \qquad \dfrac{I_{HP}}{V_I} = \dfrac{S^2/R_1}{D(s)}$ $\dfrac{V_{BP}}{V_I} = \dfrac{-S/R_1 C_1}{D(s)} \qquad \dfrac{I_{BP}}{V_I} = \dfrac{-S/R_1 R_2 C_1}{D(s)}$ $\dfrac{V_{LP}}{V_I} = \dfrac{1/R_1 R_2 C_1 C_2}{D(s)}$ $D(s) = S^2 + \dfrac{1}{R_1 C_1} S + \dfrac{1}{R_1 C_1 R_2 C_2}$ $\omega_o = \dfrac{1}{\sqrt{R_1 R_2 C_1 C_2}} \qquad Q = \sqrt{\dfrac{R_1 C_1}{R_2 C_2}}$	—
7	MOS-C Current Oscillator	12(a)	Condition of oscillation : $\dfrac{R_2}{R_1} + \dfrac{C_1}{C_2} = 1$ for $\dfrac{R_2}{R_1} = \dfrac{C_1}{C_2} = \dfrac{1}{2} \rightarrow \omega_{osc} = \dfrac{1}{R_1 C_1}$	—
8	MOS-C Floating Inductor	13	$L = \dfrac{C}{4K_1 K_2(V_{G1} - V_T)(V_{G2} - V_T)}$	—
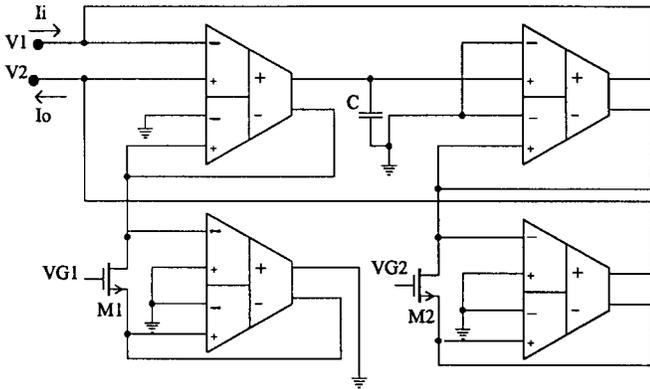
Fig. 13.   DDOFA-based MOS-C floating inductor.

G. The DDOFA-MOS-C Floating Inductor

A voltage-controlled floating inductor can also be realized by using the DDOFA and MOS transistors operating in the nonsaturation region. The MOS-C floating inductor circuit is shown in Fig. 13. The input and output currents of the circuit are equal and are given by

$$I_i = I_o = \frac{4K_1 K_2(V_{G1} - V_T)(V_{G2} - V_T)}{SC}(V_1 - V_2). \qquad (48)$$

Therefore, the circuit realizes a voltage-controlled floating inductor of magnitude given by

$$L = \frac{C}{4K_1 K_2(V_{G1} - V_T)(V_{G2} - V_T)}. \qquad (49)$$

V. CONCLUSION

A wide-range differential difference operational floating amplifier has been proposed. The DDOFA is realized using a new NMOS differential difference transconductor with large signal-handling capability. Applications of the DDOFA in analog signal processing have

been discussed, and are summarized in Table III. It is interesting to note that in all applications, tuning can be achieved via control voltage as discussed in the grounded and floating resistors, multiplier/divider cell, continuous-time filter, current oscillator, floating inductor, and also the voltage-to-current converter if a voltage-controlled grounded resistor is used. PSPICE simulation results for all applications are given to confirm the analytical results.

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An Arithmetic Free Parallel Mixed-Radix Conversion Algorithm

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Abstract— A new, parallel mixed-radix (MR) conversion algorithm, based upon lookup tables, with no required arithmetic is presented. When pipelined, an effective conversion rate of one conversion per table lookup is achieved. The new algorithm is attractive for hardware implementation since it requires no arithmetic or logical units. The alogrithm is shown to be faster than existing pipelined algorithms.

Index Terms— Mixed-radix conversion, parallel lookup, pipeline processing, residue number system.

I. Introduction

The residue number system (RNS) has been used extensively and effectively in digital signal processing. For example, see [2], [5], and [7], as well as [11] and its references. This is because, as is well-known, integer arithmetic can be naturally and efficiently parallelized by utilizing the residues of integer operands with respect to a convenient set of moduli. As is equally well-known, the mixed-radix (MR) number system is superior to the RNS for sign determination, magnitude comparison, and overflow detection. Consequently, considerable effort has been directed toward developing fast algorithms for residue to MR representation conversion.

The residue to MR representation conversion problem can be easily stated. Given relatively prime moduli $1 < m_1 < m_2 < \cdots < m_N$ and an integer $x, 0 \leq x < m_1 m_2 \cdots m_N$, x can be uniquely represented as $x = a_1 + a_2 m_1 + a_3 m_1 m_2 + \cdots + a_N m_1 m_2 \cdots m_{N-1}$, where the MR digits a_i satisfy $0 \leq a_i < m_i$. Let x have residues $x_i = x \bmod m_i$. Given the residue representation $(x_1, x_2, \cdots, x_N)$, the conversion problem consists of deriving the MR representation $(a_1, a_2, \cdots, a_N)$ quickly and efficiently. Once the MR digits are known, x itself may of course be readily recovered. (In fact, x may often be accumulated while the MR digits are being determined.) The residue to x or residue-to-decimal conversion problem has received considerable attention and many particular schemes have been proposed, though they all rely upon the Chinese Remainder Theorem or MR conversion [3]–[5].

The MR conversion problem (and more generally, the residue-to-decimal conversion problem) has an interesting history. The classical algorithm of Szabo and Tanaka [1] has been extensively utilized. It can be effectively pipelined, but it requires a considerable amount of arithmetic and significant communication between successive computations. In an effort to increase efficiency for high-speed computing, fast, inherently parallel algorithms have been presented by Huang [8], and Chakraborti *et al.* [10]. We present here a novel parallel algorithm for MR conversion, which possesses advantages over other algorithms discussed to date. When pipelined, it can achieve an effective conversion time equal to the time required for