Low Voltage Wide Range CMOS Differential Voltage Current Conveyor and its Applications

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Abstract

This paper presents a novel CMOS differential voltage current conveyor based on a wide linear range transconductor with common mode detection. The differential voltage current conveyor exhibits a wide dynamic input range of ± 0.9V. It is used to realize an instrumentation amplifier, a multiple input single output filter, and a single input multiple output universal filter. PSPICE simulations of the proposed differential voltage current conveyor and its based applications are given using 0.25μm CMOS technology from TMSC MOSIS and dual supply voltages ± 1.5V.

Keywords: differential voltage, current conveyor, transconductor, filter, instrumentation amplifier

1 Introduction

Since its first introduction, by A. Sedra and K. Smith in 1970 [1], the second-generation current conveyor (CCII) has proved to be a versatile analog building block that can be used to implement numerous high frequency analog signal applications, like filters [2]-[6] and current-mode oscillators [7]. However, when it comes to applications demanding differential or floating inputs like impedance converters and current mode instrumentation amplifiers, which also require two high input impedance terminals, a single CCII block is no more sufficient. In addition, most of these applications employ floating elements in order to minimize the number of used CCII blocks. For this reason and in order to provide two high input impedance terminals, the differential voltage current conveyor (DVCC) was proposed in 1997 [8] as a four terminal device with the following properties [Fig.1]:

$$
\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{y1} \\ V_{y2} \\ I_X \\ VZ \end{bmatrix}
\tag{1}
$$

While the X terminal voltage follows the voltage difference of terminals Y1 and Y2, a current injected at the X terminal is being replicated to the Z terminal. An ideal DVCC exhibits zero input resistance at terminal X, and infinite resistance at both Y terminals as well as the Z terminal. The flow direction of the output current follows the input current direction with both currents flowing either into or out of the device. Since the DVCC exhibits two high input impedance terminals, it shows itself suitable for handling differential input signals. In addition, it has the advantage of minimizing the number of floating elements inherent in many CCII applications.
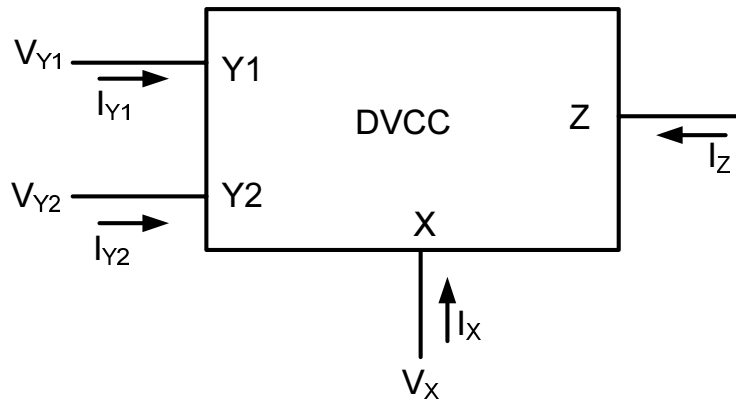

Figure 1: Block representation of the DVCC

In this paper a new wide range CMOS DVCC operating under a supply voltage of ± 1.5V is proposed. The input stage of the proposed DVCC is realized using two wide linear range transconductors. The output stage consists of a Class-AB CMOS push-pull network, which guarantees high current driving capability and low standby current. In addition, this paper proposes a new multiple input single output (MISO) filter based on the presented DVCC. Furthermore, a new single input multiple output (SIMO) universal filter with grounded elements is demonstrated. This paper is organized as follows: In section 2 the proposed wide range DVCC circuit is presented. Thereafter, DVCC applications including the MISO and the SIMO filters are discussed in section 3. PSPICE simulations for all proposed circuits are provided using 0.25μm TSMC CMOS technology.

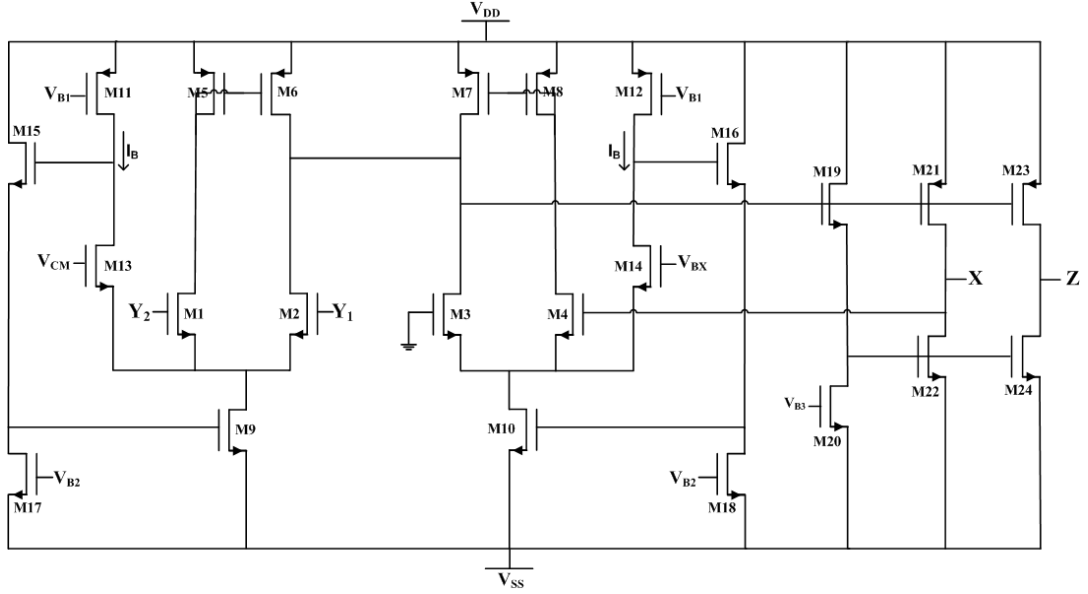# 2 Proposed DVCC CMOS Circuit Realization

A. Circuit Description

Figure 2: CMOS realization of the proposed DVCC

The circuit realization of the proposed DVCC [Fig.2] is based on equalizing the output currents of two wide linear range transconductors, formed by transistors (M1-M18). In addition, (M19-M22) comprise a Class-AB output stage, providing current swings up to ±1mA. Moreover, the current at the X terminal is transferred to the Z terminal with the aid of (M23, M24), which must be -for a unity current gain- matched with (M21, M22) respectively. All transistors are assumed to be operating in saturation.The operation of a wide linear range transconductor relies mainly on biasing a long tail differential pair LTDP (M1-M2) with a dynamic tail current ISS that increases with Vid2 where Vid = VY1 - VY2. Since the output current produced at the drains of M2 and M6 is expressed by:

$$I_{out} = I_{M1} - I_{M2} = -KV_{id}\sqrt{I_{SS}/K - (V_{id}/2)^2} \qquad (2)$$

Where K represents the transconductance parameter of M1 or M2, then if the tail current is set to:

$$I_{SS} = K[(V_{id}/2)^2 + c^2] \qquad (3)$$

A linear relation between the output current and the differential input voltage can be obtained with:

$$I_{out} = -KcV_{id} \tag{4}$$

Obviously, the value of c should be constant, which along with the transconductance parameter K is defining the overall gain of the transconductor. Concerning the dynamic input range, it is well known that the differential input voltage applied to a LTDP is limited by:

$$-\sqrt{2I_{SS}/K} < V_{id} < \sqrt{2I_{SS}/K} \tag{5}$$

Hence, in order to increase the input range of the transconductor the ratio ISS/K should be increased. Such condition is spontaneously satisfied if the tail current is dynamically increased as in equation(3), which ensures an extended differential input range. Biasing the LTDP with a constant tail current, on the other hand, will require a high ISS/K ratio. Unfortunately, this affects the minimum possible common mode input voltage, whose value must maintain the tail biasing transistor in saturation [9]. The main concern now is how to realize equation(3) . Considering the differential pair currents, they are given by:

$$I_{M1} = \frac{K}{2}(V_{Y2} - V_S - V_T)^2 \tag{6}$$

$$I_{M2} = \frac{K}{2}(V_{Y1} - V_S - V_T)^2 \tag{7}$$

So taking into account that the input signals of a differential pair can be divided into a common mode voltage (VCM) and a differential voltage (Vid) with VY1 = Vid/2 +VCM and VY2 = -Vid/2 +VCM where VCM = (VY1+VY2)/2, then the tail current can be expressed by:

$$I_{SS} = I_{M1} + I_{M2} = K[(\frac{V_{id}^2}{2}) + (V_{CM} - V_S - V_T)^2] \tag{8}$$

Obviously, ISS will follow the function given in equation(3), if the subsequent expression is set to a constant value:

$$V_{CM} - V_S - V_T = c \tag{9}$$

A simple source follower (M13), whose gate is connected to the common mode voltage of the LTDP, and whose source is clamped to the differential pair coupled source, can be used to satisfy equation(9). In this case, the source follower should have a constant drain current, set by M11, so that c is equal to:

$$c = \sqrt{\frac{2I_B}{K_{13}}} \tag{10}$$

As a consequence, the current equations result into:

$$I_{M1} = \frac{K}{2}(-\frac{V_{id}}{2} + \sqrt{\frac{2I_B}{K_{13}}})^2 \tag{11}$$

$$I_{M2} = \frac{K}{2}(\frac{V_{id}}{2} + \sqrt{\frac{2I_B}{K_{13}}})^2 \tag{12}$$

$$I_{ss} = K[(\frac{V_{id}}{2})^2 + \frac{2I_B}{K_{13}}] \tag{13}$$

$$I_{out} = -K\sqrt{\frac{2I_B}{K_{13}}}V_{id} \tag{14}$$

$$I_{M9} = I_{SS} + I_B = K[(\frac{V_{id}}{2})^2 + I_B(\frac{2}{K_{13}} + \frac{1}{K})] \tag{15}$$

From the previous equations, the standby current of M1 and M2 is defined by the value 2IB/K13. For differential input voltages greater than twice the square root of 2IB/K13 M1 turns off and the current flowing in M2 increases. On the other hand, as the differential input voltage is decreased below twice the square root of 2IB/K13, M2 turns off and the current flowing in M1 increases. In both cases, M9 should feed the necessary current required for proper operation of M1 and M2 even if it enters slightly in the linear region. Therefore, the problem with the minimum common mode input voltage required to maintain the tail biasing transistor in saturation has less effect in this circuit. Furthermore, since both M1 and M2 are 'ON' at standby, this circuit exhibits low distortion. It should be also noted, that the current flowing in M9 will change by feedback action, formed by M15, in order to stabilize the value of VS. In addition, the dynamic differential input range is extended to:

$$-2\sqrt{2I_B/K_{13}} < V_{id} < 2\sqrt{2I_B/K_{13}} \tag{16}$$

Consequently, the compromise between the differential input voltage range and the LTDP standby current limits the performance of the transconductor. Concerning VCM, if the input voltages are fully differential or balanced, VCM is a constant value that can be applied directly to the gate of M13. Otherwise, a common mode detection circuit like the one shown in fig.3 is used to track VCM. For proper operation of the common mode detection circuit, all transistors should be working in saturation mode, while M25-M28 should be matched. The input dynamic range of this circuit is limited by:

$$-2\sqrt{2I_B/K_{25}} < V_{id} < 2\sqrt{2I_B/K_{25}} \tag{17}$$

Moving back to the DVCC circuit, the voltage follower is implemented by connecting the outputs of two identical transconductors, producing the following

total current at the drain of M2:

$$Iout1 + Iout2 = K\sqrt{\frac{2I_B}{K_{13}}}[-(V_{Y1} - V_{Y2}) + (V_X - 0)] = 0 \qquad (18)$$

In consequence, the voltage at the X terminal follows the voltage difference of terminals Y1 and Y2. This condition is valid as long as both output currents are linear, which is guaranteed over a wide range when using the proposed transconductor. Concerning the gate voltage of M14, it should follow the common mode voltage of the input signals applied to M3 and M4. As these inputs are neither fully differential nor balanced, a common mode detection circuit becomes essential for the second transconductor, producing $V_{BX}=V_X/2$.

Figure 3: Common Mode Detection Circuit

B. Simulation Results

The performance of the proposed COMS DVCC was verified by performing PSPICE simulations with supply voltages ±1.5V using 0.25μm TSMC CMOS technology. Simulations were carried out using balanced input voltages with transistor aspect ratios given in table I. Fig.4 presents the X and Z voltages versus the differential input voltage, when the proposed DVCC is used to realize a unity gain amplifier with 5kΩ load resistance. The DVCC shows good linearity for differential input voltages between ±0.9V, with a total standby power dissipation of 1.74mW. In fig.5 the magnitude response of the DVCC with a differential voltage ac-varying signal of 0.5V magnitude and open-circuited output terminals is demonstrated. The DVCC shows a flat response with 85MHz 3-dB BW. The input and output referred noise spectral

densities are then displayed in fig.6. Thereafter, the Z terminal output current versus the X terminal input current is shown in fig.7 with a 1mA linear range, while the variation of the offset voltage across the X terminal with grounded Vid is illustrated in fig.8. The X terminal input resistance RX is less than 9Ω and the offset voltage doesn't exceed 8.2mV. Fig.9 clarifies the push-pull action of the Class-AB output stage with a standby current of 136 μA. Moreover, the magnitude response of the DVCC with an ac-varying input current of 10μA magnitude and a short-circuited Z terminal is displayed in fig.10. The DVCC provides a 120MHz 3-dB bandwidth. The time response to a 1MHz differential square input voltage is tested in fig.11, resulting in a rise time in the vicinity of 7.5ns. Finally, the total harmonic distortion is evaluated for different differential input voltage amplitudes [Fig.12]. A 1MHz sinusoidal input generates a THD factor less than 0.009. The power supply rejection ratio (PSRR) from the positive supply to the output has a value of 41.27dB and from the negative supply to the output is 50.3dB. Table II compares the performance parameters of the proposed DVCC with a DVCC employing constant tail current (omitting M11-M18, and the common mode detector circuit). The proposed circuit exhibits a 1.50 wider voltage range on the expense of a 49μW power increase, and a 0.39 BW loss.
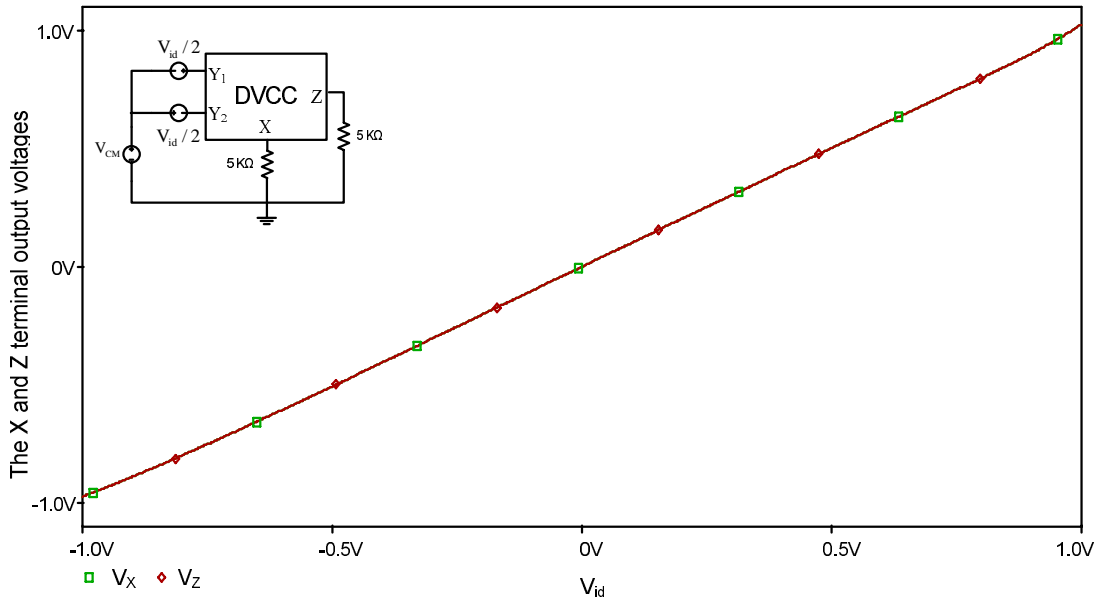
Figure 4: The X and Z terminal output voltages versus changes of Vid
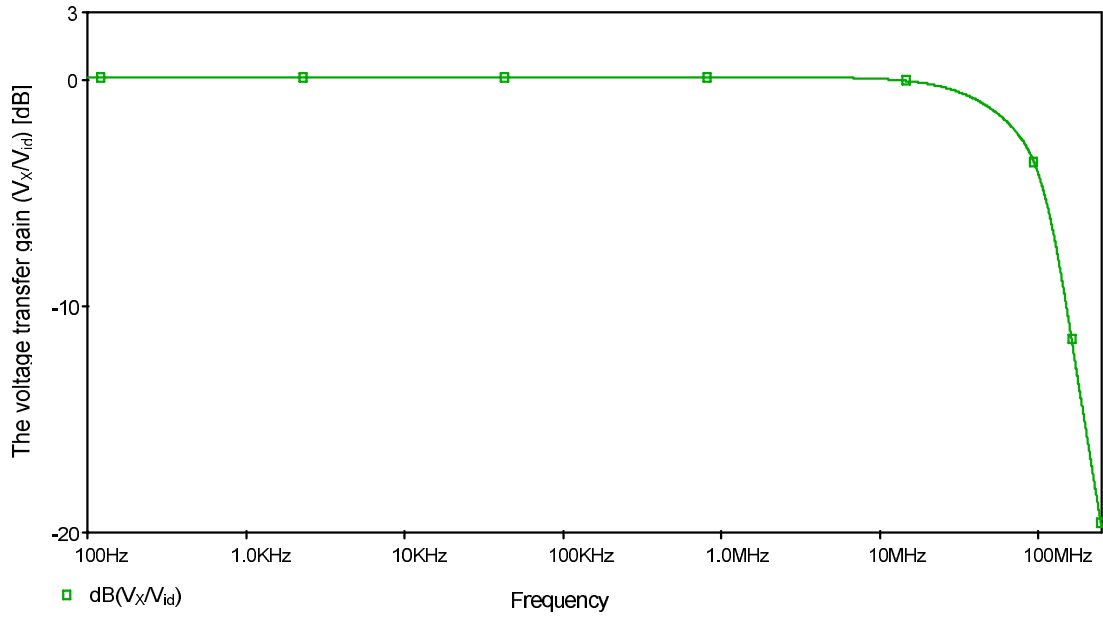
Figure 5: Magnitude frequency response of the voltage transfer gain

3   Applications Based on the Proposed DVCC

In this section the proposed DVCC is used to realize an instrumentation ampli-
fier, a new MISO second-order LP-BP filter, and a SIMO second-order univer-
sal filter. In all applications one should recognize the benefits of using differen-
tial voltage current conveyors, which focus on providing high input impedance
circuit designs with grounded elements.

A.Instrumentation Amplifier
The first basic application that can be implemented using a DVCC is an instru-
mentation amplifier as shown in fig.13. An instrumentation amplifier takes a
differential input voltage, multiplies it with a gain, and produces a single ended
output voltage. The relation between the output voltage and the differential
input can be described by the following equation:

$$V_{out} = \frac{R_2}{R_1} V_{id} \tag{19}$$
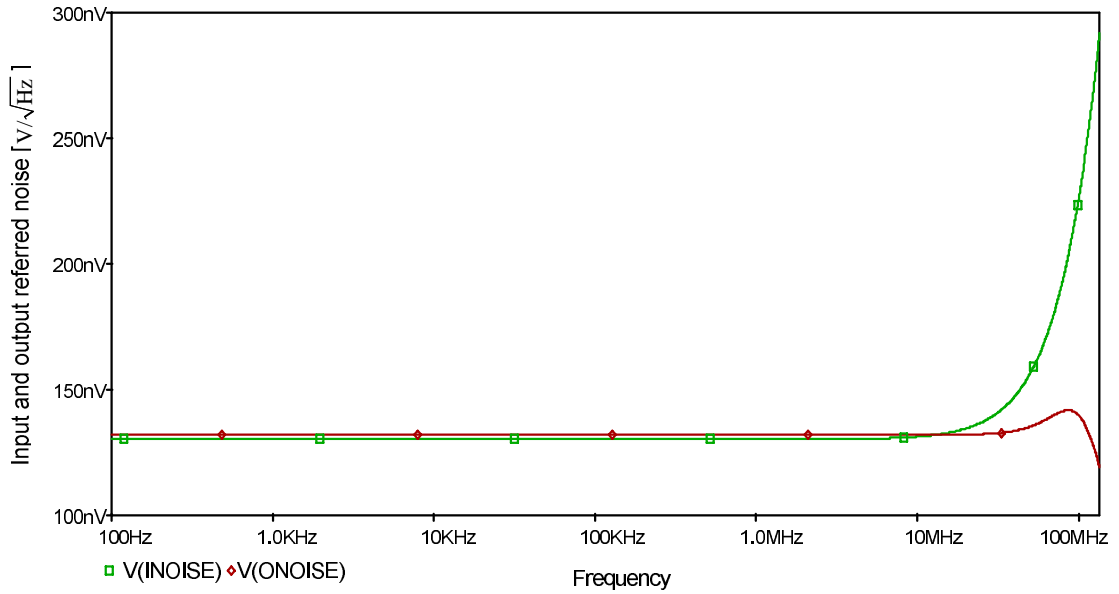
Figure 6: Input and output voltage referred noise spectral densities

Obviously, the ratio of the Z terminal resistance to the X terminal resistance defines the gain G of the amplifier. In addition, this circuit can realize an inverting or noninverting amplifier, by simply connecting Y1 or Y2 to ground, respectively. One should also note that this circuit can be utilized as a voltage-controlled voltage source (VCVS). In order to verify the performance of the instrumentation amplifier, PSPICE simulations were carried out using 1.5V supply voltages. The X terminal resistance was set to 2kΩ, while the Z terminal resistance was scanned from 2kΩ to 8kΩ in steps of 2kΩ. The length of the output stage transistors was increased to 0.75μm to minimize the channel length modulation effect. Fig.14 displays the DC gain of the instrumentation amplifier for G varying from 1 to 4, while fig.15 is demonstrating the ac gain. The 3-dB BW proves to be constant for different gain values.

B.Multiple Input Single OutputBP-LP Filter

In this section the proposed DVCC is used to realize a MISO second-order LP-BP filter as shown ind fig.16. Two different responses are achieved depending on the actual active input. If the first input is active, while the second one is grounded, an inverting bandpass response is obtained. On the other hand, grounding the first input while activating the second one generates a noninvert-
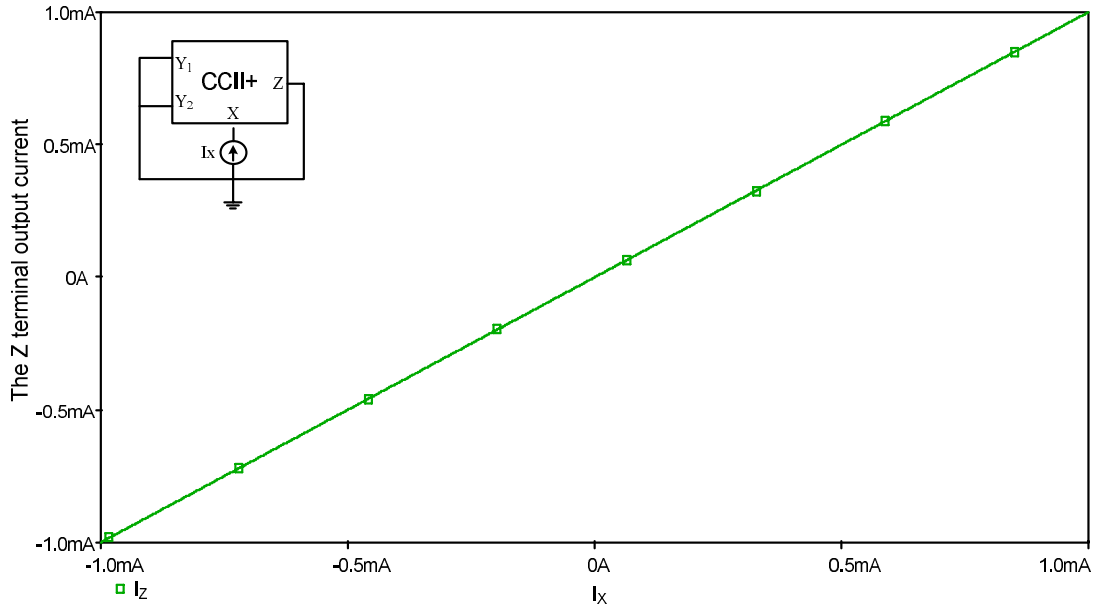
Figure 7: The Z terminal output current versus changes of IX

ing lowpass response. This can be verified through direct analysis, obtaining the following transfer equations and gains:

$$\frac{V_o}{V_1} = -\frac{\frac{S}{C_1 R}}{D(S)} \tag{20}$$

$$\frac{V_o}{V_2} = -\frac{\frac{1}{C_1 C_2 R_2 R}}{D(S)} \tag{21}$$

$$D(S) = S^2 + \frac{S}{R_1 C_1} + \frac{1}{C_1 C_2 R_2 R} \tag{22}$$

$$A_{vBP} = -\frac{R_1}{R} \tag{23}$$

$$A_{vLP} = 1 \tag{24}$$

From equation (22), ω_o and Q and of the filter are given by:

$$\omega_o = \sqrt{\frac{1}{C_1 C_2 R_2 R}} \tag{25}$$

$$Q = R_1 \sqrt{\frac{C_1}{C_2 R_2 R}} \tag{26}$$
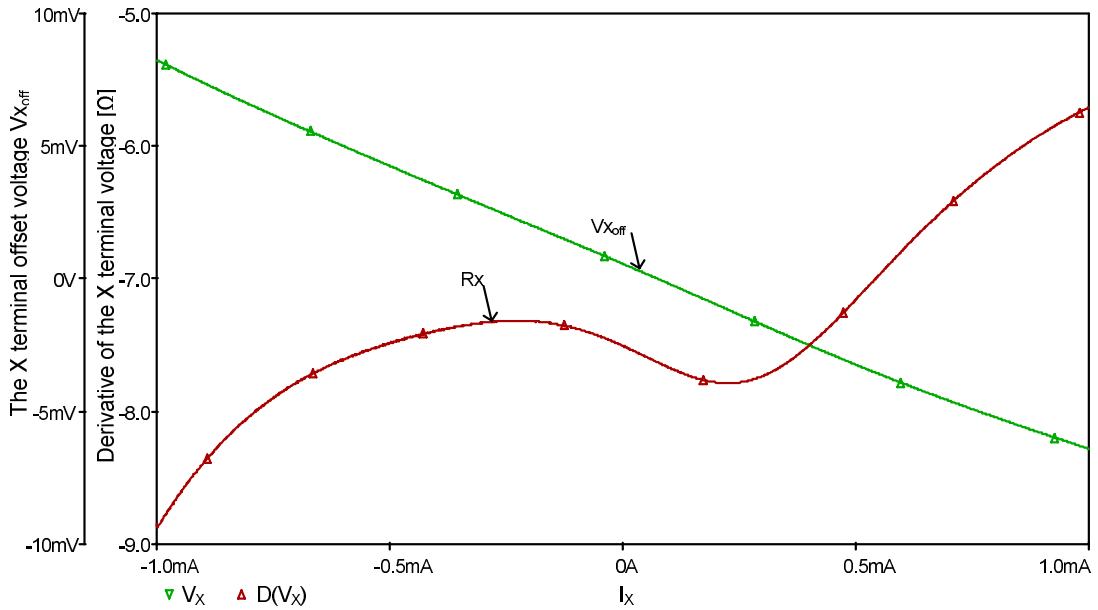
Figure 8: The offset voltage of the X terminal along with its derivative

Simulation results prove the aforementioned relations with passive element values given in table III. In fig.17 a lowpass response is generated by grounding V1 and applying an ac varying signal at V2. The cutoff frequency is around 465kHz, which is very close to the theoretical value. Next, the bandpass response is tested by grounding V2 and injecting the ac varying signal at V1. The passive elements values were optimized as shown in table III to achieve a banpass filter with a 7.4 quality factor Q and a 690kHz center frequency fo [Fig.18].

C.SIMO Filter

The filter configuration presented in fig.19 realizes a single input multiple output universal filter with noninverting HP, BP and LP outputs. This filter employs four DVCC blocks, two grounded capacitors, and five grounded resistors. The first two input blocks operate as a summer and the last two are integrators, with their outputs fed back to the input DVCC blocks. This configuration, which resembles the CFOA based filter proposed in [10], provides several advantages over the typical active filters with CFOA. First, it has infinite input and output impedances. Second, all elements are grounded. By applying direct analysis to the filter blocks, the following transfer functions
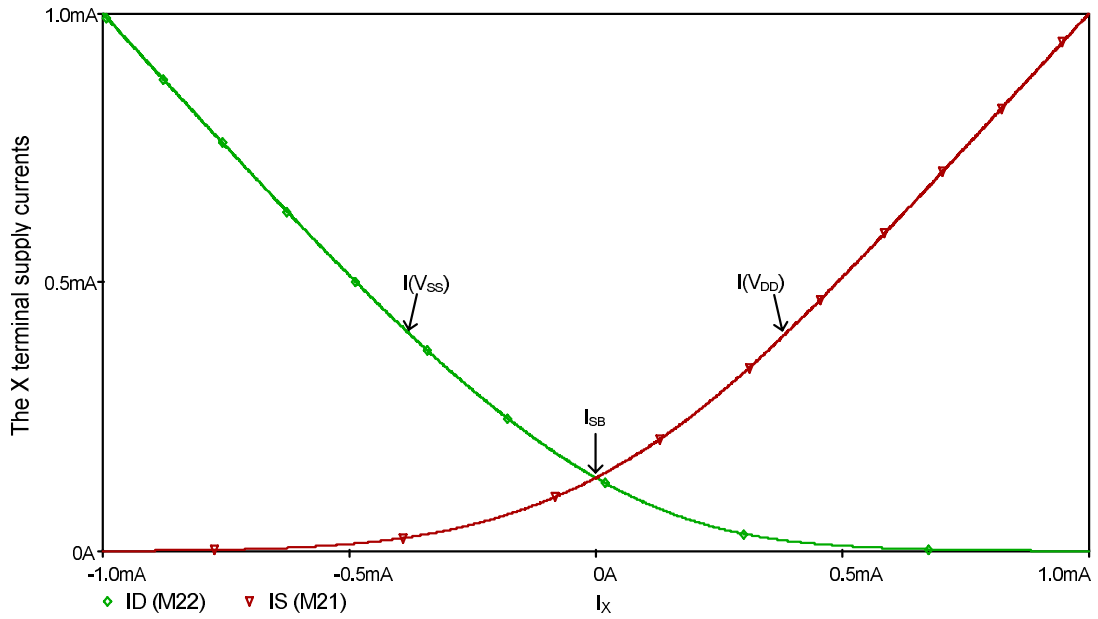
Figure 9: Driving capabilities of the output stage

and gains are obtained:

$$\frac{V_{HP}}{V_i} = \frac{\frac{S^2 R(R_3+R_4)}{R_3 R_4}}{D(S)} \tag{27}$$

$$\frac{V_{BP}}{V_i} = \frac{\frac{SR(R_3+R_4)}{R_1 C_1 R_3 R_4}}{D(S)} \tag{28}$$

$$\frac{V_{LP}}{V_i} = \frac{\frac{R(R_3+R_4)}{R_1 C_1 R_2 C_2 R_3 R_4}}{D(S)} \tag{29}$$

$$D(S) = S^2 + S\frac{R}{C_1 R_1 R_4} + \frac{R}{C_1 C_2 R_1 R_2 R_3} \tag{30}$$

$$A_{vHP} = \frac{R(R_3 + R_4)}{R_3 R_4} \tag{31}$$

$$A_{vBP} = 1 + \frac{R_4}{R_3} \tag{32}$$

$$A_{vLP} = 1 + \frac{R_3}{R_4} \tag{33}$$

From equation (30), ωo and Q and of the filter are given by:

$$\omega_o = \sqrt{\frac{R}{R_1 R_2 R_3 C_1 C_2}} \tag{34}$$
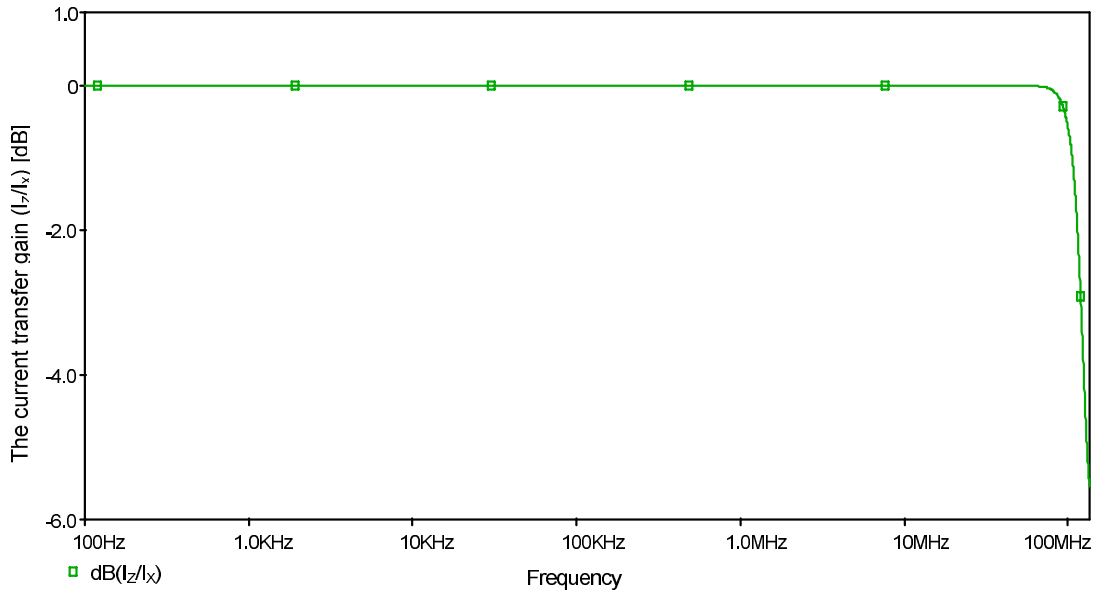
Figure 10: Magnitude frequency response of the current transfer gain

$$Q = R_4\sqrt{\frac{R_1C_1}{RR_2R_3C_2}} \tag{35}$$

Fig.20 shows the simulated highpass and lowpass frequency responses with the design parameters given in table IV. The simulated cutoff frequency equals to 469 kHz which is very close to the theoretical value. The design parameters are then optimized as shown in table IV to achieve a bandpass response with Q = 8 and fo = 800kHz [Fig.21].

4   Conclusion

In this paper, a novel CMOS differential voltage current conveyor based on a wide linear range tranconductor has been presented. The DVCC has demonstrated a wide dynamic range in the vicinity of 0.9V for the voltage follower and a 1mA for the current follower. The DVCC was used to implement an instrumentation amplifier, a MISO LP-BP filter, and a SIMO universal filter. The proposed DVCC circuit and the realized applications have been verified using PSPICE simulations.
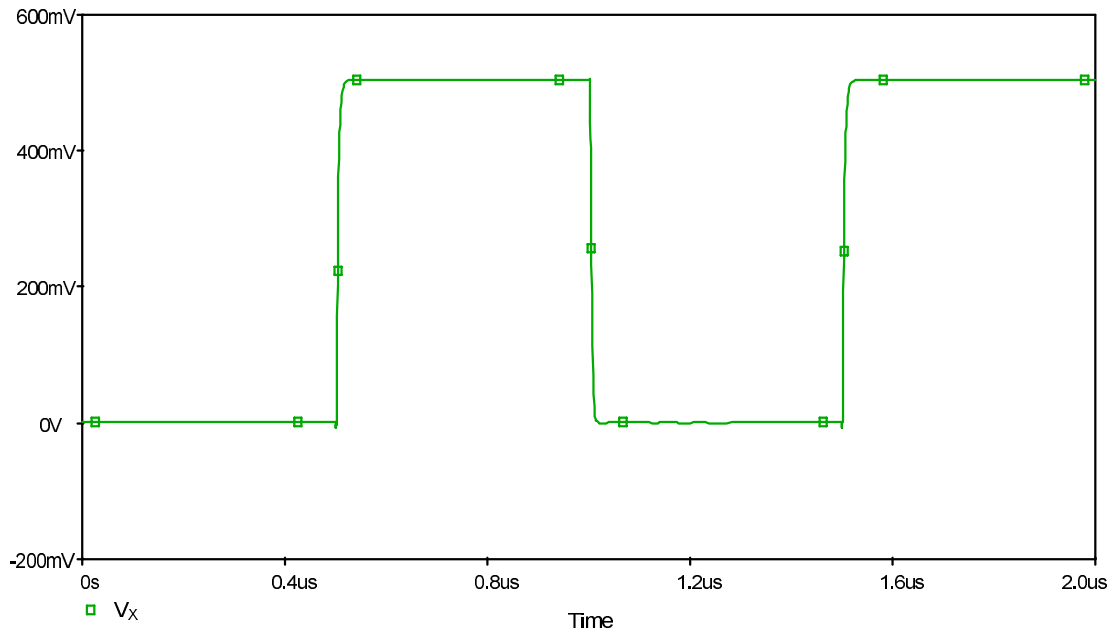
Figure 11: The X terminal voltage along with a 0.5V-1MHz differential square input

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Table 1: Transistor Aspect Ratios For The Proposed DVCC

Transistors	W(μm)	L(μm)
M1-M4	0.5	4
M5-M8	1	1
M9-M12,M19-M20,M25-M28	0.5	0.5
M13-M14	0.5	1
M15-M16	5	0.5
M17-M18	1	0.5
M21-M24	20	0.25
M29-M30	6	2
M31-M32	5	2

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Table 2: Performance Comparison For The Proposed DVCC

Parameter	$\frac{Proposed}{DVCC}$	$\frac{ConstantTailcurrent}{DVCC}$
CMOS Technology	0.25μm	0.25μm
Power supply (VDD,VSS)	(1.5V,-1.5V)	(1.5V,-1.5V)
No. of transistors	32	16
Total power dissipation	1.74mW	1.25mW
Tail Current	Dynamic	10μA
Standby current of the output stage(ISB)	136μA	136μA
PSRR$^+$	41.27dB	34.56dB
PSRR$^-$	50.3dB	50.1dB
Input dynamic range with the X terminal resistance 5KΩ	-0.9V to 0.9V	-0.4V to 0.4V
Voltage transfer error	0.00136	0.00237
Current driving capability	$\pm$1mA	$\pm$1mA
Current transfer erroe	0.0013	0.0051
X terminal offset voltage with Y and Z are ground	8.2mV	24mV
X terminal input resistance	9Ω	32Ω
X terminal open circuit BW	85MHz	137MHz
Z terminal short circuit	120MHz	250MHz
X terminal THD@ Vid=0.2sin 2Πf	0.0013@1MHz	0.0069@1MHz
Rise time/fall time(pulse 0.25V@1MHz)	7.48ns/6.24ns	3.2ns/3.1ns
Input referred noise	130nV/$\sqrt{Hz}$	94.64nV/$\sqrt{Hz}$
Input referred noise	132nV/$\sqrt{Hz}$	94.56nV/$\sqrt{Hz}$

Table 3: Passive Elements of The MISO Filter

Response $\frac{LPF}{Elements}$	Value	$\frac{BPF}{Elements}$	Value
R, R$_1$-R$_2$	1KΩ	R	2KΩ
C$_1$	0.25nF	R$_1$	0.65KΩ
C$_2$	0.5nF	R$_2$	0.5KΩ
		C$_1$	0.8nF
		C$_2$	0.2nF

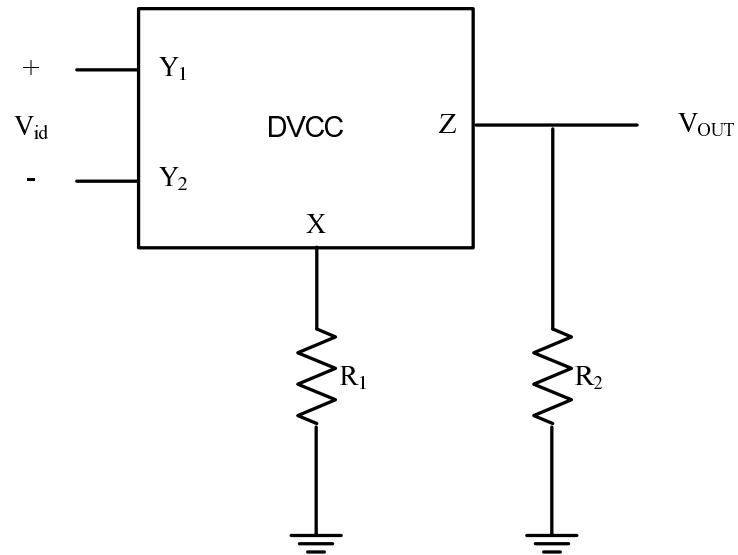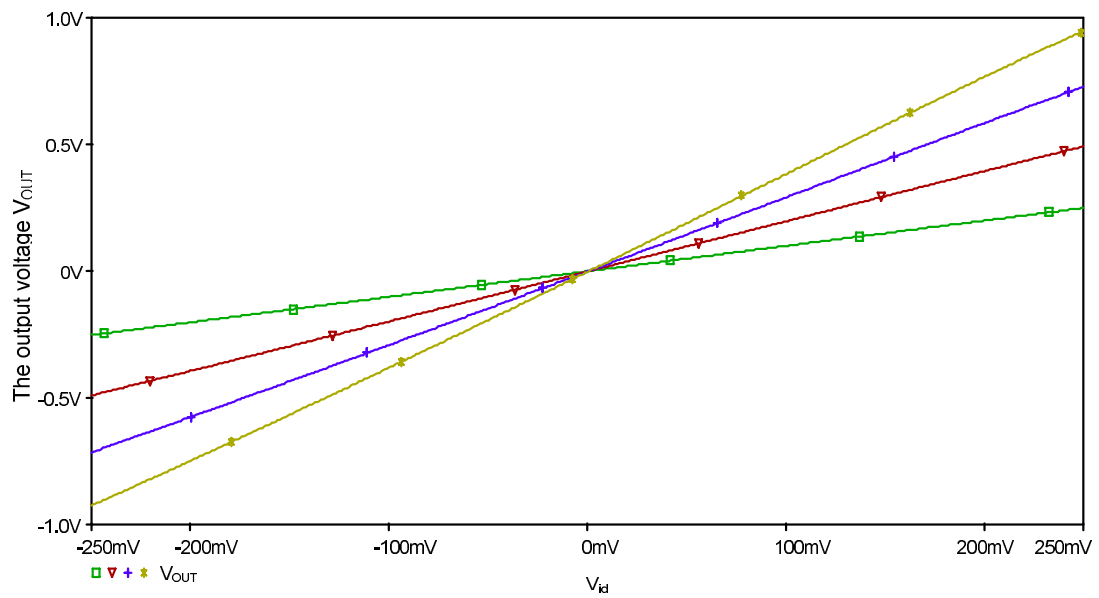Figure 12: X terminal total harmonic distortion (for frequencies 100kHz and 1MHz)

Figure 13: Circuit realization of the instrumentation amplifier

Figure 14: DC transfer characteristics of the instrumentation amplifier (G = 1 to 4)
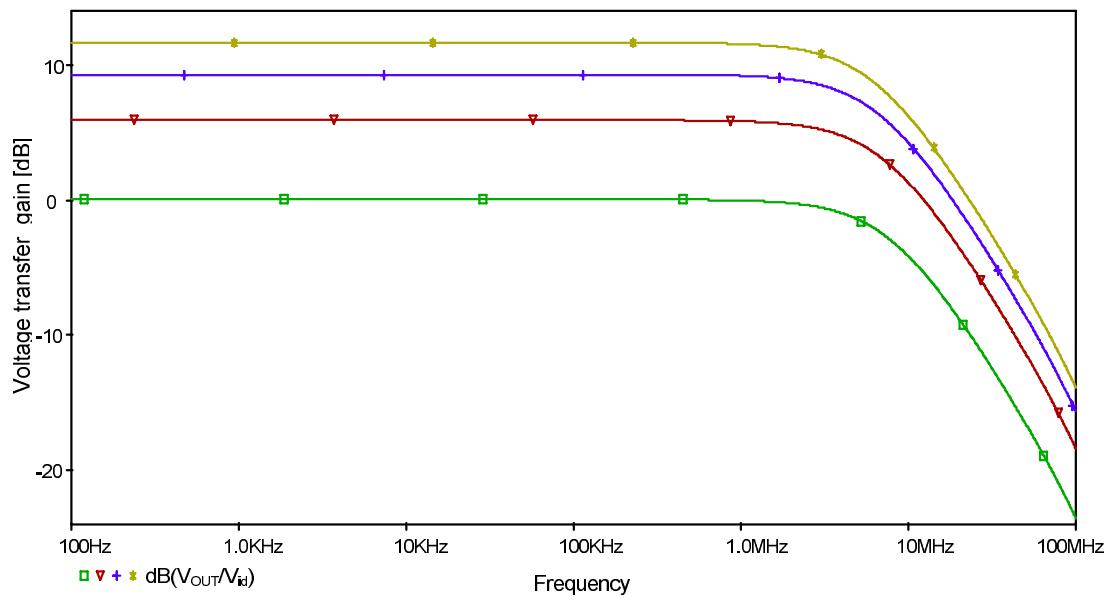
Figure 15: Magnitude frequency response of the instrumentation amplifier (G = 1 to 4)

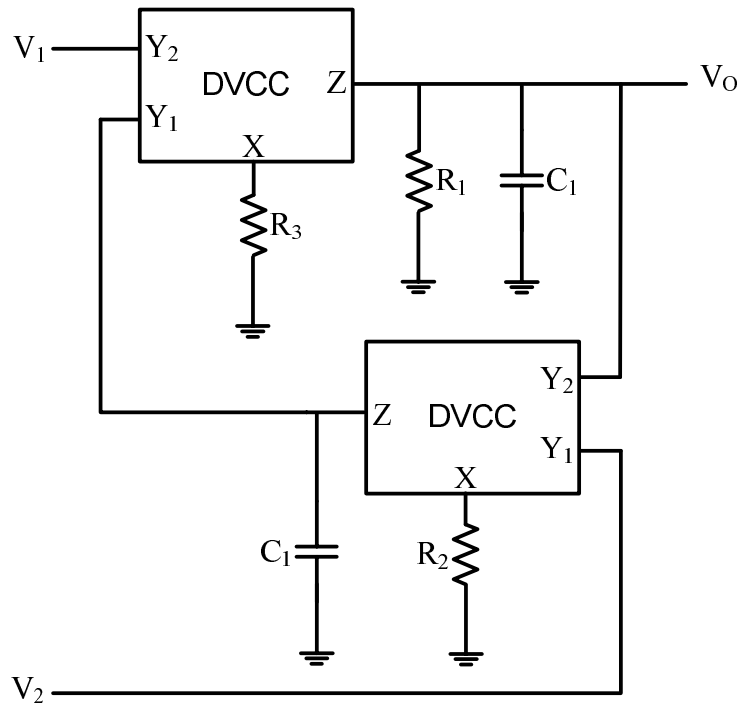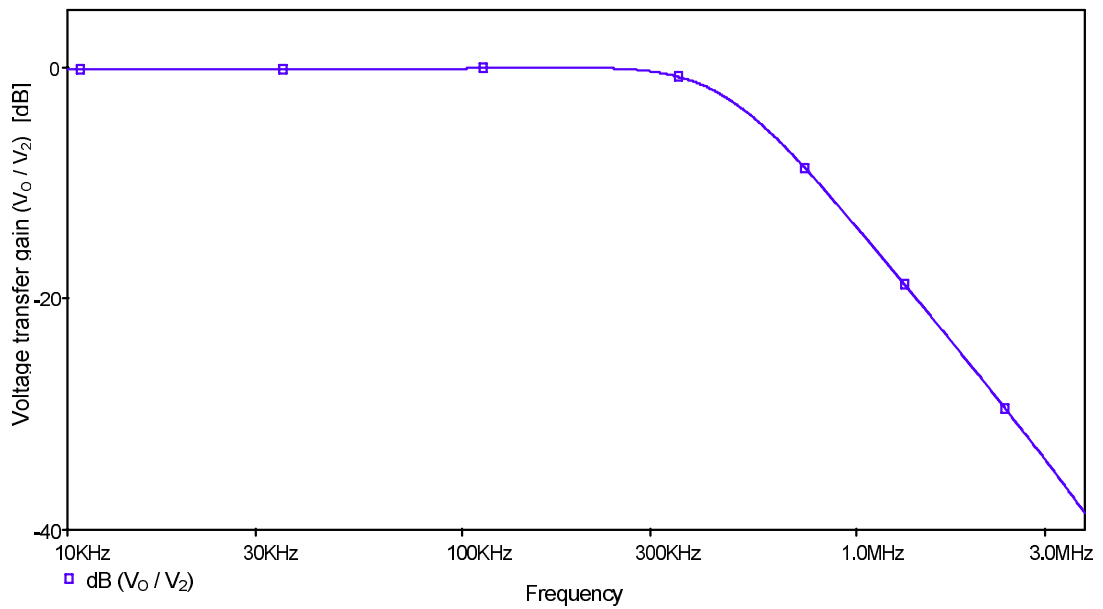Figure 16: Circuit realization of the MISO filter

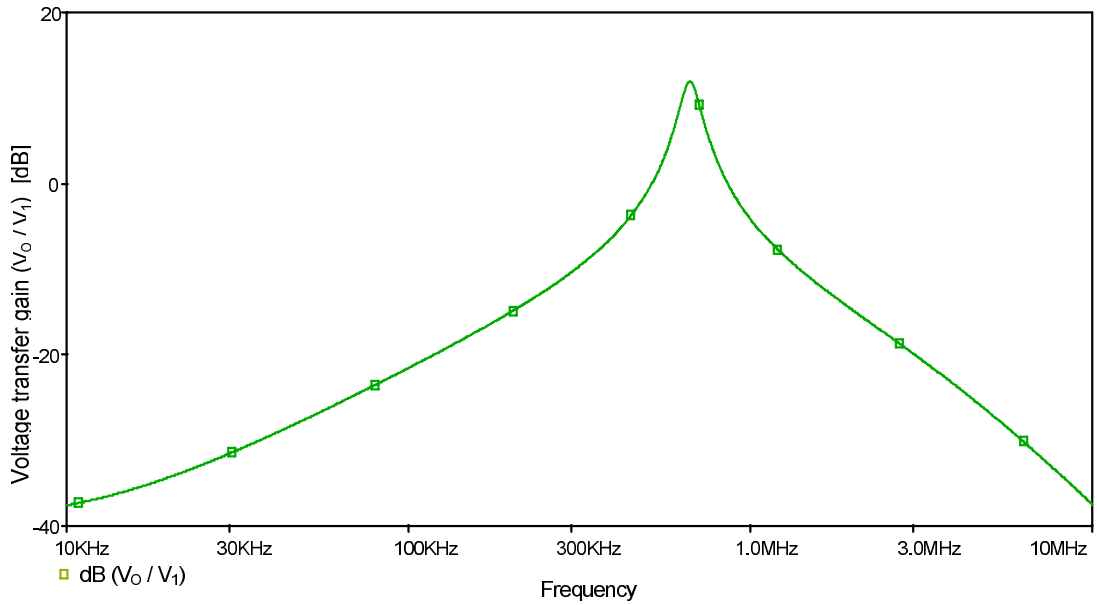Figure 17: LP magnitude frequency response of the MISO filter

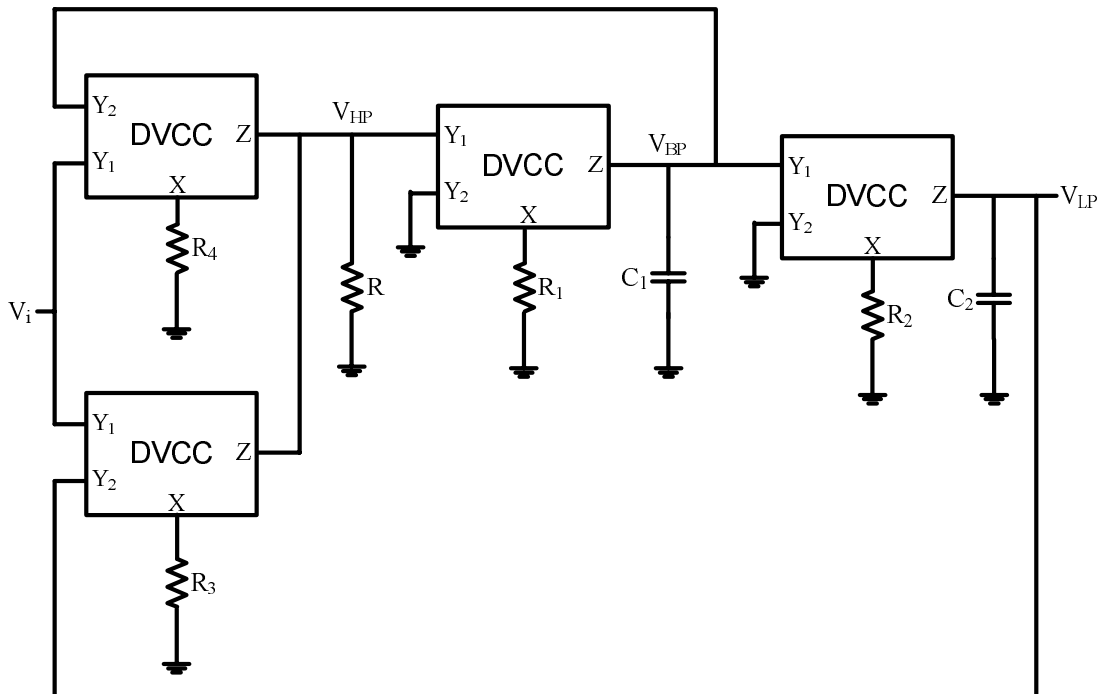Figure 18: BP magnitude frequency response of the MISO filter

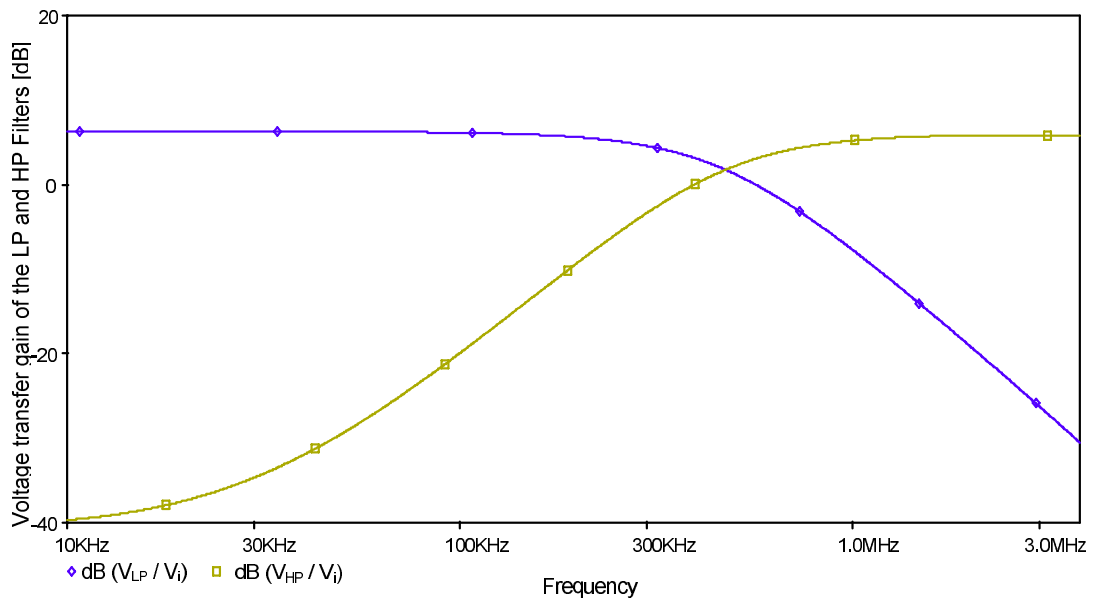Figure 19: Circuit realization of the SIMO universal filter

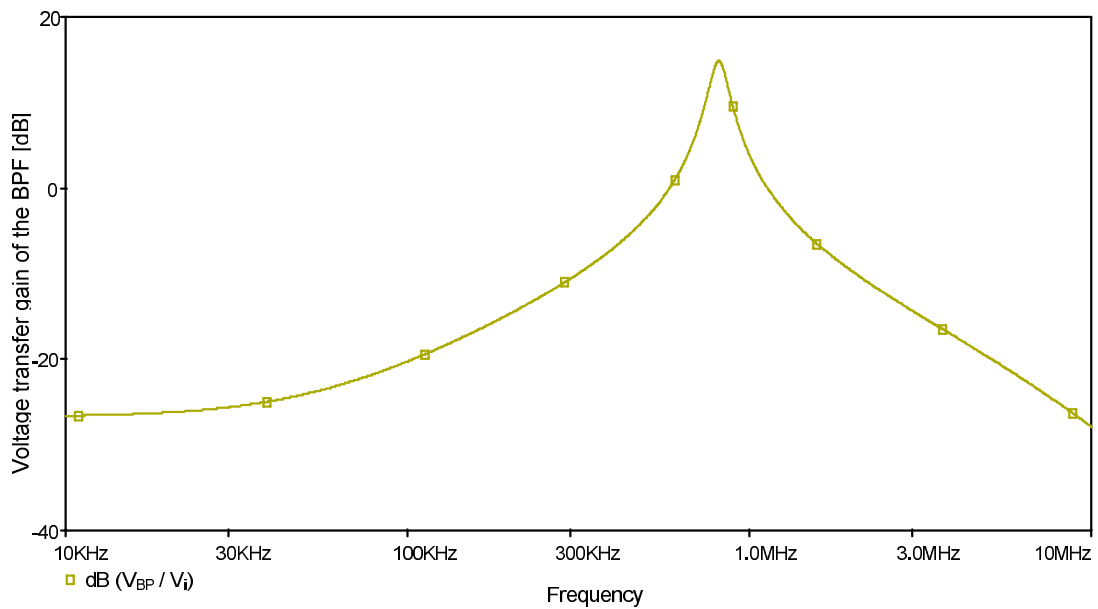Figure 20: LP and HP magnitude frequency responses of the SIMO filter

Figure 21: BP magnitude frequency response of the SIMO filter