Design of Low-Power K-Band Circuits in CMOS Technology

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Abstract

Millimeter-wave (mm-wave) CMOS transceivers have attracted interest in recent years, especially in the 24 GHz and 60 GHz ISM bands. As indispensable building blocks in a wireless transceiver, frequency generation and conversion circuits are confronted by many design challenges. At mm-wave frequencies, the voltage controlled oscillator (VCO) suffers from a poor phase noise and a limited tuning range, while the frequency divider is usually accompanied by a narrow locking range and high power consumption. Direct down-conversion mixer, on the other hand, suffers from a very poor noise figure as a result of the flicker noise. For the generation of the LO signals with low power consumption, the design of the VCO encounters difficulties. Moreover, the generation of IQ signals with high accuracy over a wide band is much more challenging.

In this dissertation, new techniques and optimized topologies are proposed to improve the performance of mm-wave frequency generation and conversion circuits. Employing a transformer feedback topology, a 24 GHz LC-VCO was designed using 130 nm CMOS technology. It achieves a wide tuning range and consumes one fourth of the power that the conventional LC-VCO requires. The designed transformer feedback VCO has comparable phase noise to the conventional counterpart. Two designs of the mm-wave frequency divider have also been presented. One design is a Ka-band Miller frequency divider in 130 nm CMOS technology. A specific optimization approach was followed to achieve a maximum locking range for low power consumption. The loop gain is maximized over the widest possible frequency range, the Q factor of the load inductor, on the other hand, is chosen such that the third order harmonic is rejected by a required predetermined value. Measurement results of the designed circuits show that their performance compares to the state-of-the-art developments and satisfies the 24 GHz FMCW radar application.

The other design is a 45 GHz static frequency divider using 90 nm CMOS technology. New techniques such as “inductive peaking”, “split resistors”, and “asymmetric sizing of input transistors” are employed to minimize the power consumption of the divider. Moreover, direct down-conversion mixer is designed. Overcoming the flicker noise effect was a challenge. Novel current bleeding network was therefore proposed. Not only the noise performance is improved but the conversion gain is increased as well. Based on the designed static frequency divider and the direct down-conversion and up-conversion mixers, complete IQ-modulator and demodulator were eventually implemented using 90 nm CMOS technology. Measurement results of the designed and tested circuits show that their performance compares to the state-of-the-art developments and satisfies the 60 GHz high-data-rate communication application of the IEEE 802.15.3c standard.